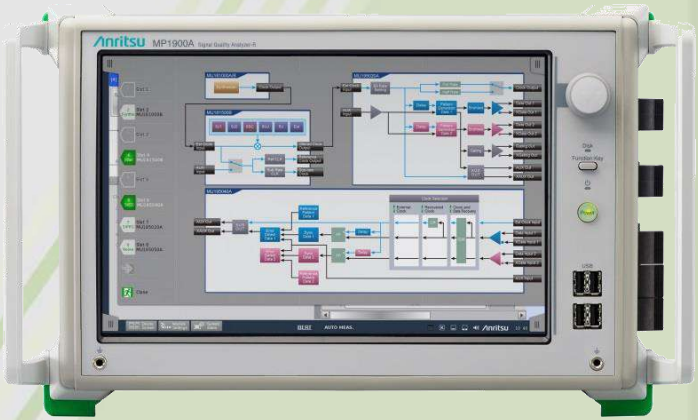
Anritsu Advancing beyond

# Signal Integrity Analysis
# Multi-channel High-Performance BERT

## Signal Quality Analyzer-R
## MP1900A Series

SQA-R



# Outline

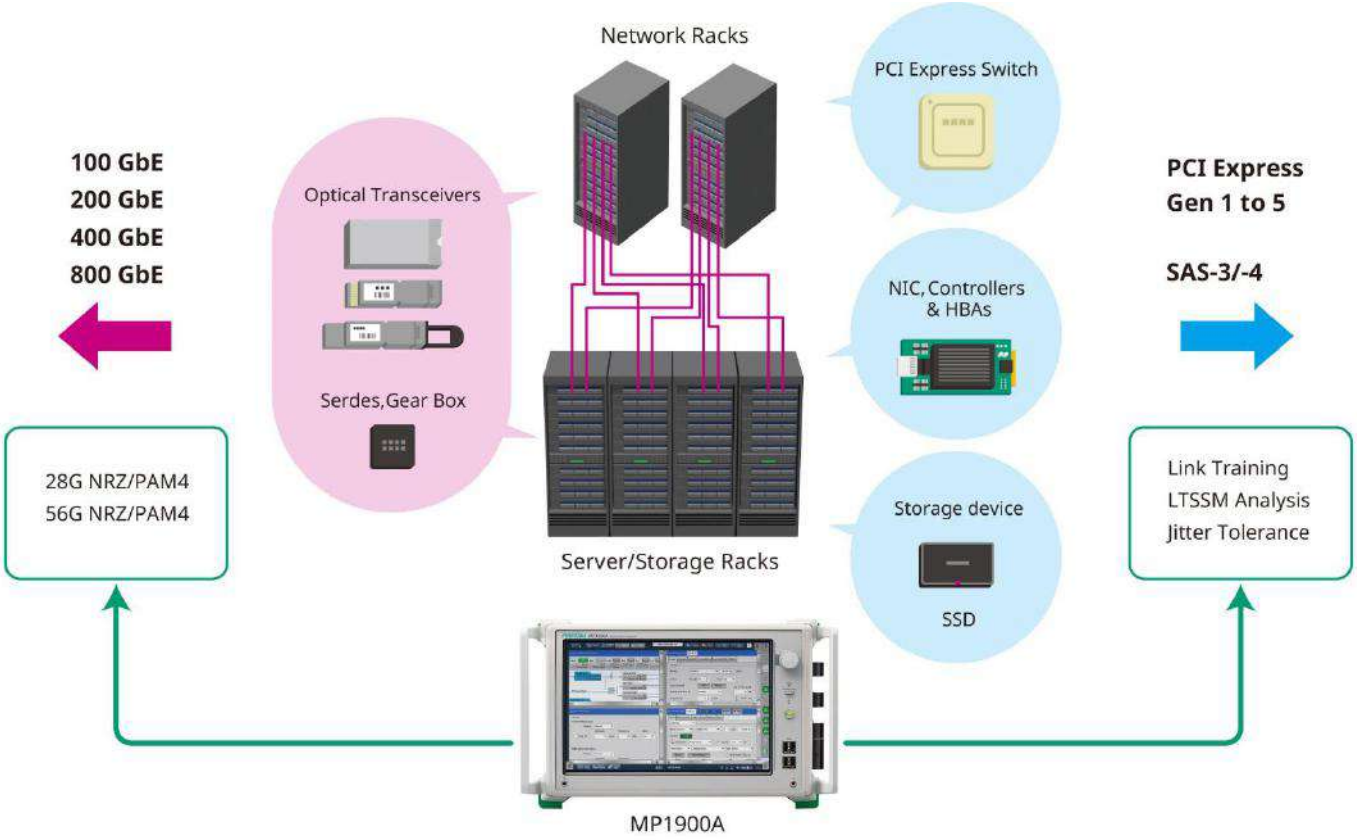
- Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, data centers are transitioning network interfaces to faster 200/400/800 GbE standards, and PCI bus interconnects speeds now exceed 10G. In addition, support for multi-channels is also increasing transitioning.
- The Signal Quality Analyzer-R MP1900A series is an 8-slot modular type, high-performance BERT with excellent expandability supporting measurement applications by installing 32 Gbit/s Multi-channel PPG/ED, 64 Gbaud PAM4 PPG/ED and Jitter/Noise addition modules for signal integrity analysis of increasingly faster devices. Moreover, as well as functions for evaluating the Physical layer of high-speed interfaces, the built in Link Training/LTSSM analysis function supports all in one measurement of high-speed network interfaces such as 400/800 GbE, and bus interfaces such as PCIe.

**MP1900A Series Supported Applications**

100 GbE/200 GbE/400 GbE/800 GbE, CEI-25G/28G/56G/112G,
InfiniBand EDR/HDR/NDR, Fibre Channel
PCI Express Gen1 to 5, USB 3.2/USB4, Thunderbolt 3, SAS-3/SAS-4, DP1.4
Optical Module, SERDES, AOC, High-Speed Interconnect

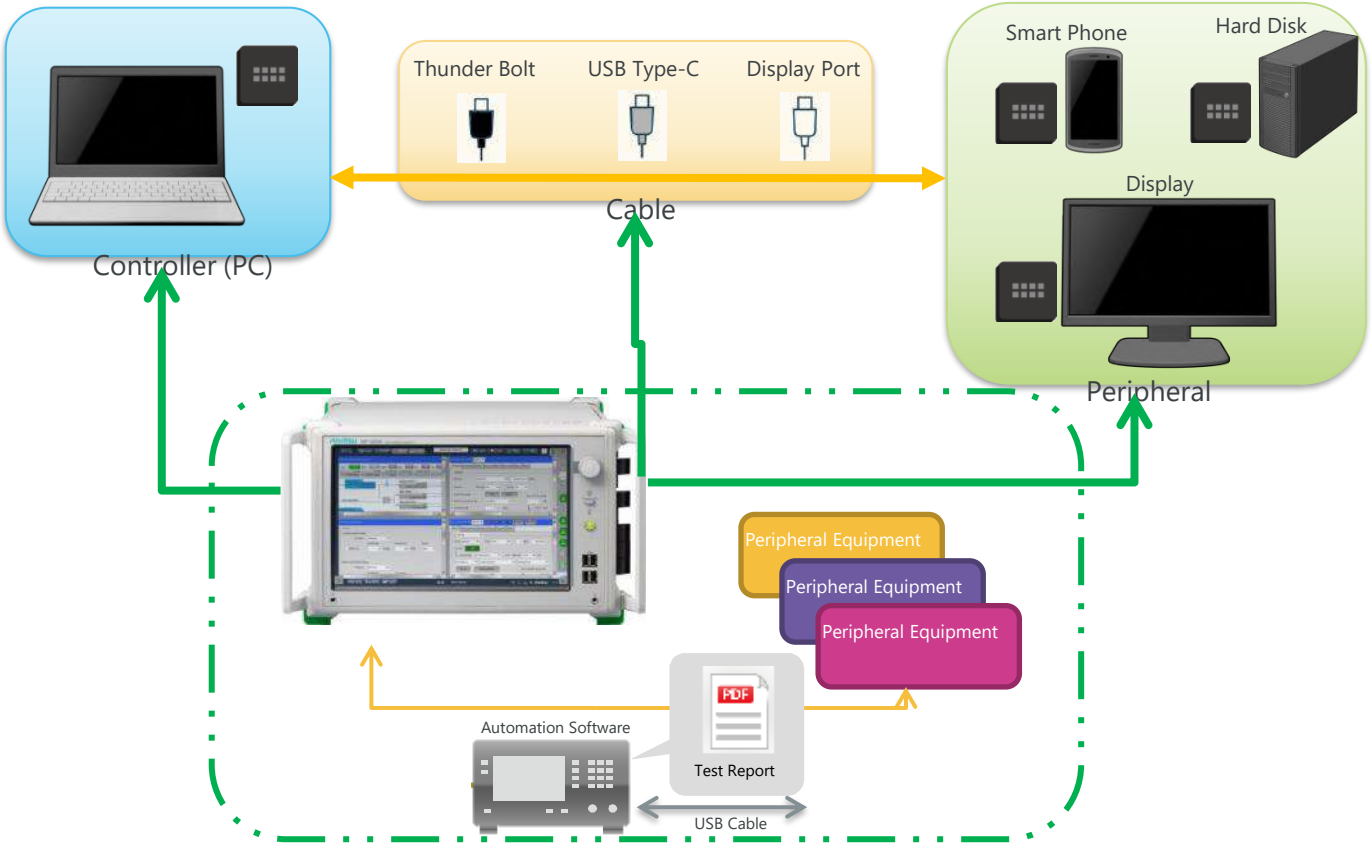
# MP1900A Update Points [1]

The MP1900A series is a high-expandability, high-performance BERT supporting physical layer evaluations of high-speed interfaces. The all-in-one design covers early stage R&D evaluations ranging from next-generation 400/800 GbE network interfaces to PCI Express, etc., bus interfaces.



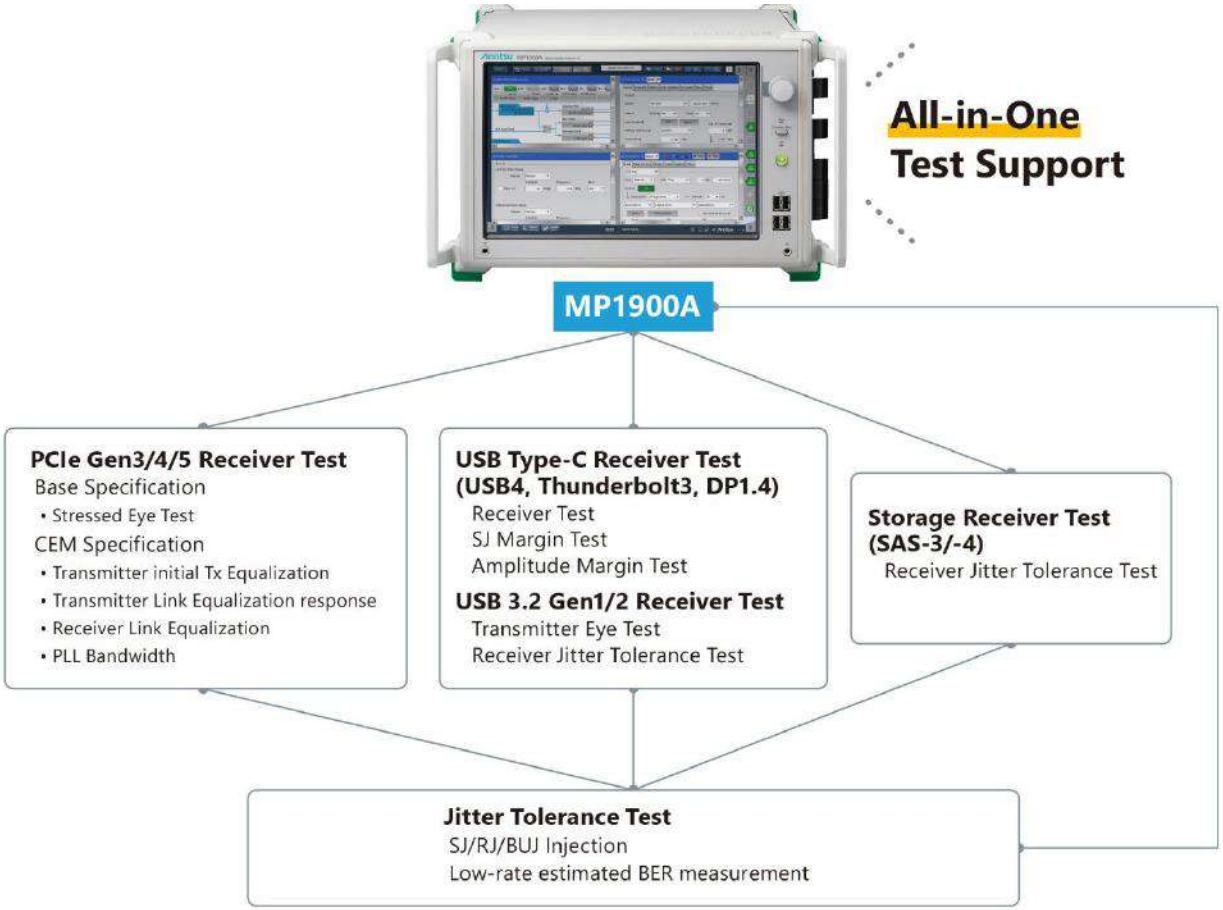
# MP1900A Update Points [2]

With the increase in various serial-bus interface speeds linking PCs and peripherals, quality can only be assured by accurate Physical layer evaluations.
The MP1900A with integrated application software controls peripheral equipment to accurately and quickly perform the measurements required by each standard.



# Multi-IF Support

Supports IF speeds over wide bandwidth from 2.4 Gbit/s to 21 Gbit/s with expandability to 32 Gbit/s without hardware upgrades; one unit enables Rx tests for PCIe Gen5 (32 GT/s), USB Type-C (USB4(20 Gbit/s) , Thunderbolt3(20 Gbit/s)) , DisplayPort1.4(8.1Gbit/s)) and SAS-4(22.5 Gbit/s).



# MP1900A Series Features

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## Excellent expandability

- 8 slots (per one MP1900A main unit)
- Maximum transmission capacity up to 512 Gbit/s (supporting up to 16ch of 32 Gbit/s NRZ, 4ch of 64 Gbaud PAM4)
- All-in-one support for both high-speed network interfaces such as 400/800 GbE and bus interfaces such as PCIe

## Full support for high-speed device signal integrity evaluations

- Bit rates of 2.4 Gbit/s to 32.1 Gbit/s (NRZ, SI PPG/ED series)
  2.4 Gbaud to 64.2 Gbaud (128.4 Gbit/s) (PAM4, PAM4 PPG/ED series)
- Built-in Emphasis and Equalizer
- Low Intrinsic Jitter data output 115 fs rms (typ., SI PPG)
- High input sensitivity 15 mV (Eye Height) (typ., SI PPG)
- Built-in Clock Recovery
- Jitter (SJ/RJ/BUJ/SSC) and noise (CM/DM/White) tolerance measurements

## All-in-one coverage of next-generation digital interface Rx tests

- Supports PCIe Gen1 to Gen5, SAS-3/-4, USB Type-C interface (USB3.2/USB4/Thunderbolt3), and DisplayPort1.4.
- Link Negotiation and LTSSM analysis functions
- Automated test-signal calibration and receiver tests

# Supports Wideband & Multi-channel Measurement Requirements

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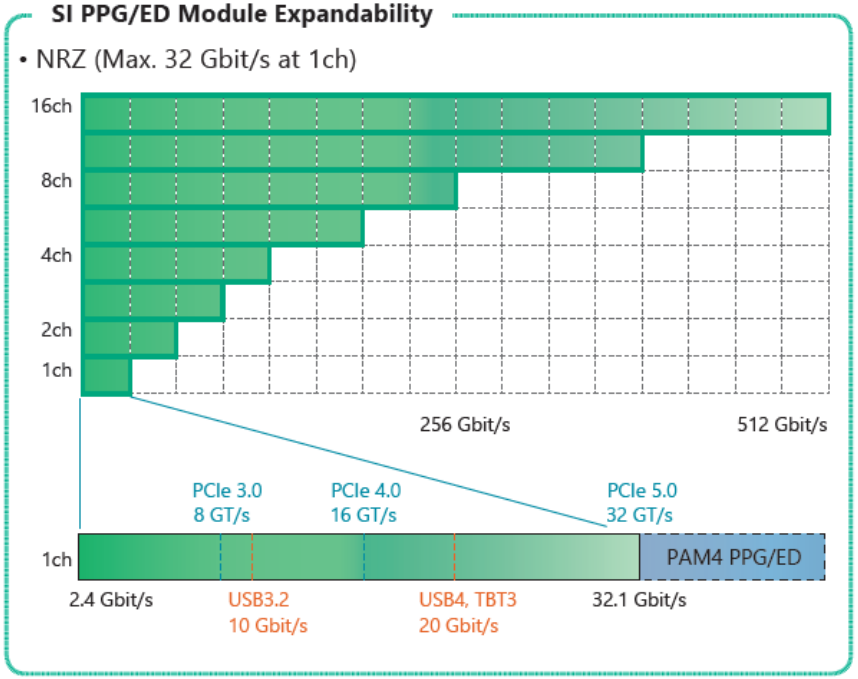
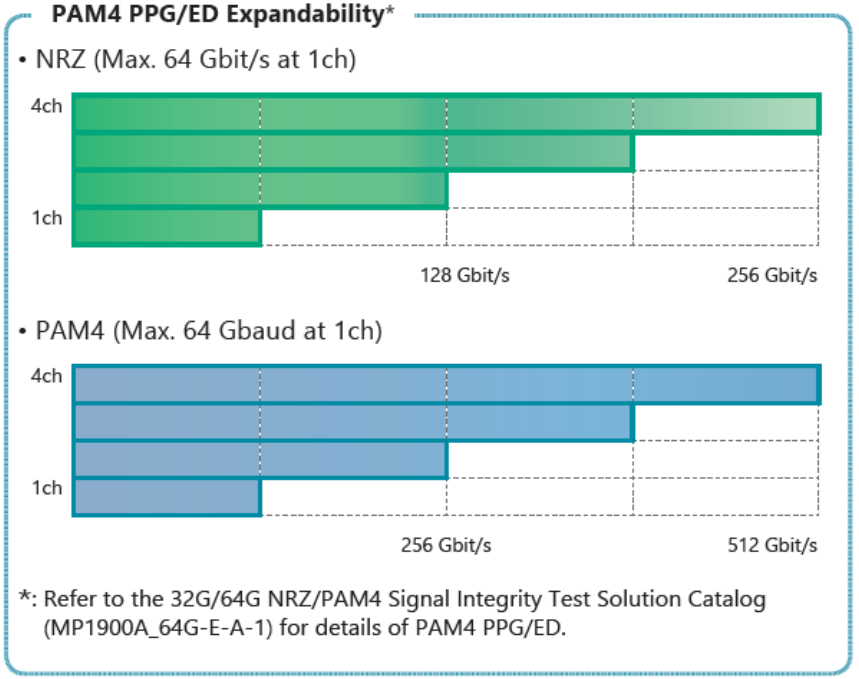
The 8-slot modular type Signal Quality Analyzer-R MP1900A can be easily customized to support more measurement channels and new required functions and performance without wasting previous investments in equipment. With cost-effective upgrade support for next-generation interfaces, such as 400/800 GbE, the MP1900A will play a key role in bringing customers' products more quickly to market .



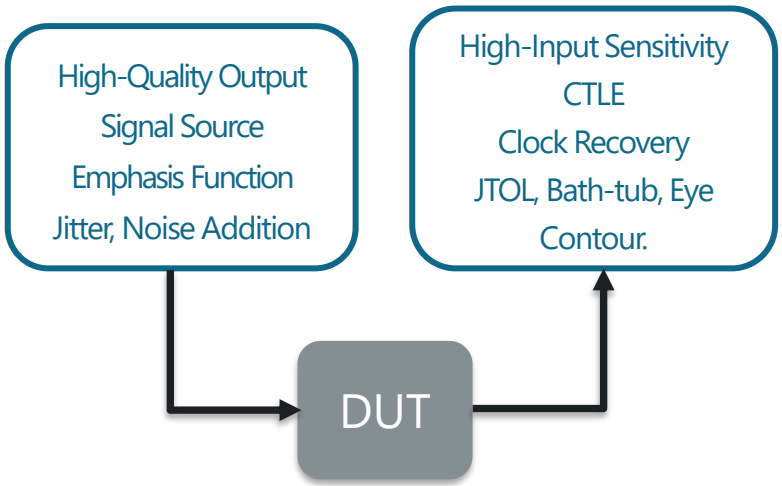



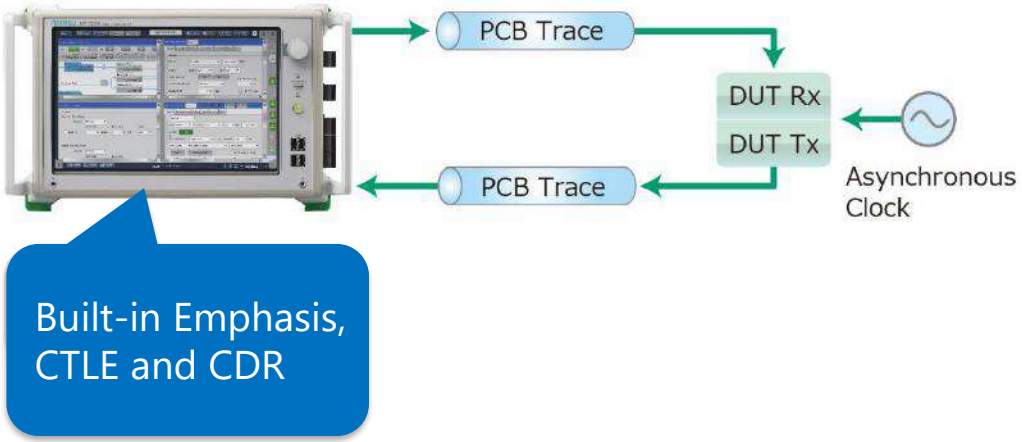
# Ideal for Signal Integrity Evaluations (1/2)

The 21G/32G bit/s SI PPG MU195020A has a built in 10Tap (max.) Emphasis option for simulating various devices and channels as well as for outputting corrected waveforms reproducing channel-path losses to help improve design evaluation efficiency.

The Rx-side 21G/32G bit/s SI ED MU195040A has a built in multi-band CTLE (Continuous Time Linear Equalization) function supporting 28, 16, and 8 Gbit/s band input signals for performing BER measurements of Eyes closed by transmission path losses. Since this CTLE function is a hardware equalizer rather than software emulator, it supports evaluation of TRx BER performance under near-to-live conditions, such as BER evaluation of test signals, and comparison of DUT BER measurement results.

**Signal Integrity Evaluations**
**Required Performance and Functions**



# Ideal for Signal Integrity Evaluations (2/2)

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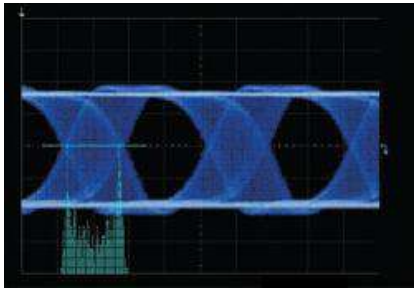
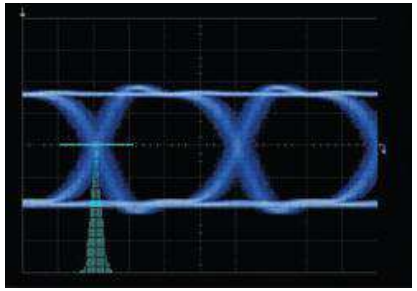
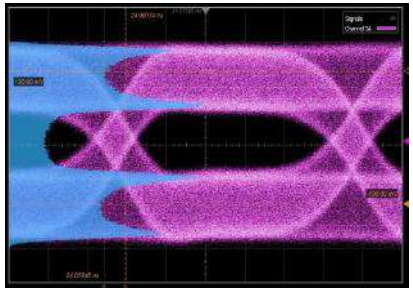
To perform high-speed receiver stressed input tolerance tests, the BER is measured under the worst conditions using a stressed signal with added jitter and voltage noise. Using the MP1900A series with the Jitter Modulation Source MU181500B, Noise Generator MU195040A with CDR function for adding various Jitter types and SSC and the Jitter Tolerance Test MX183000A-PL001 software, supports receiver tolerance tests in conformance with the various interface standards. The MP1900A series offers strong support for receiver stressed input tolerance tests by high-quality output signal before jitter and noise addition and high-linearity jitter and noise addition functions.



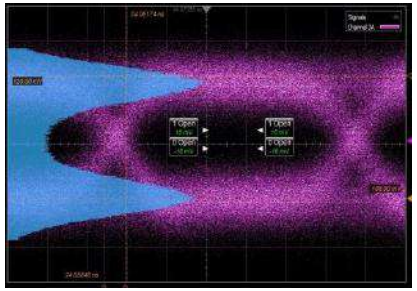
Sinusoidal Jitter(SJ)



Random Jitter(RJ)



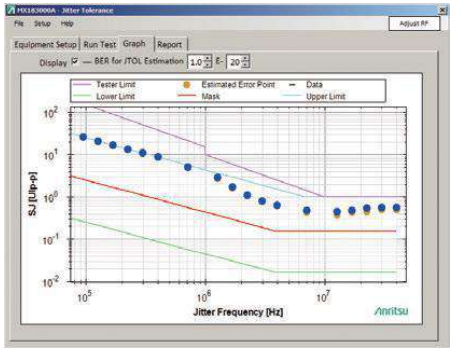
CM/DM Noise



White Noise

**Jitter Tolerance Test Function (MX183000A-PL001)**

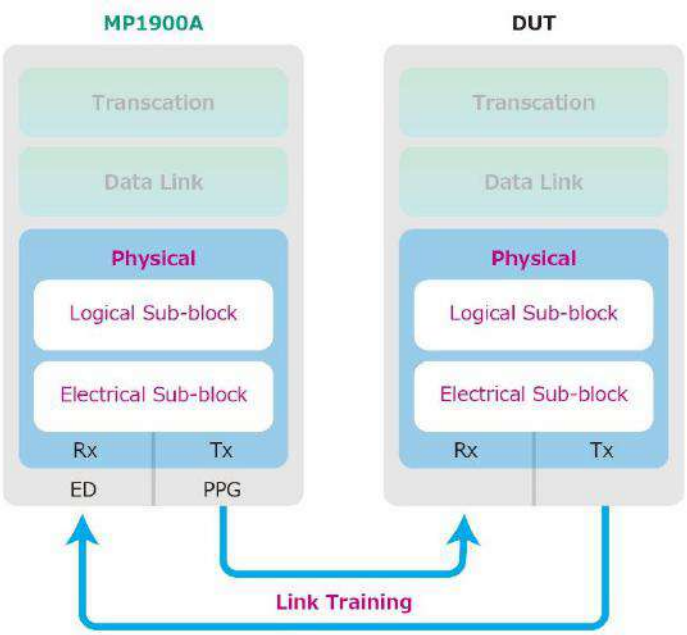
- High-versatility Jitter Tolerance measurements
- PHY Device Jitter Tolerance tests by impressing SJ/RJ/BUJ
- Standards-compliant Mask measurements
- Fast measurement times using low error rate estimation function, such as 1E–12 and 1E–15
- Tolerance measurements versus device characteristics using four Binary, Upward, Downward, Binary + Linear methods




Low Error Rate Estimation Jitter Tolerance Measurements

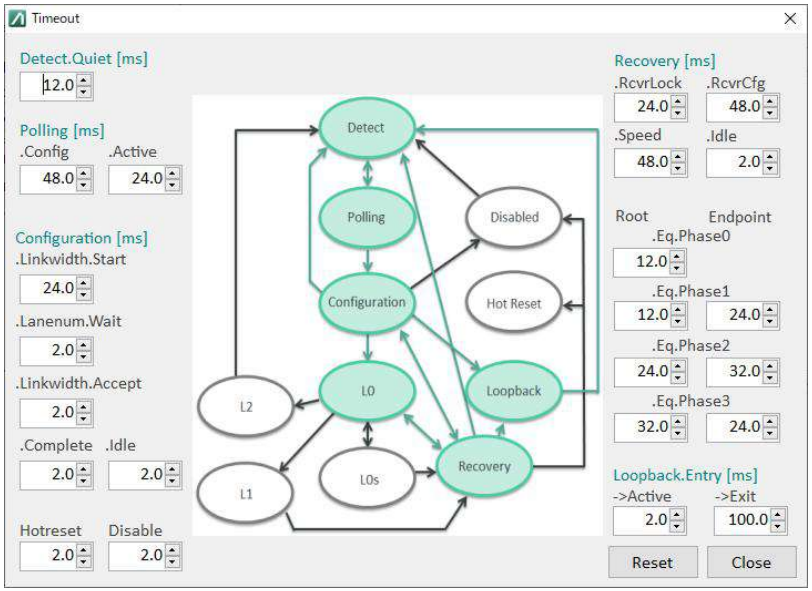
# Built-in PCI Express Link Training and LTSSM Analysis Functions

High-speed serial interfaces require good interconnectivity between devices and equipment, and it is important to identify whether a dropped Link is caused by physical or logical errors. The all-in-one MP1900A series supports Physical layer evaluations for PCIe Gen1 to Gen5 and future Gen6 receivers, in addition to having Link Training for securing normal operation, also has functions for detecting and analyzing LTSSM (Link Training Status State Machine) fault transitions to improve detection efficiency.




Supports physical layer measurements of add-in cards and system boards

- Tx/Rx Link Equalization Response Test
- Rx Link Equalization Test
- Receiver Jitter Tolerance Test

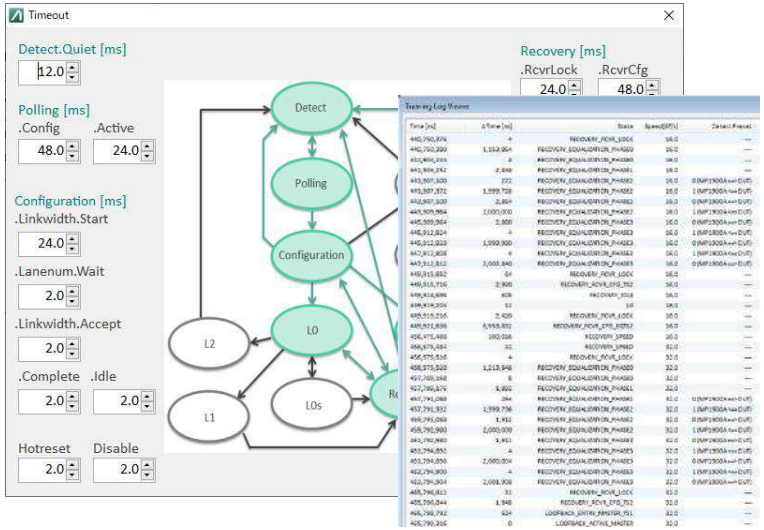



PCI Express Link Training State transitions (MX183000A-PL021)

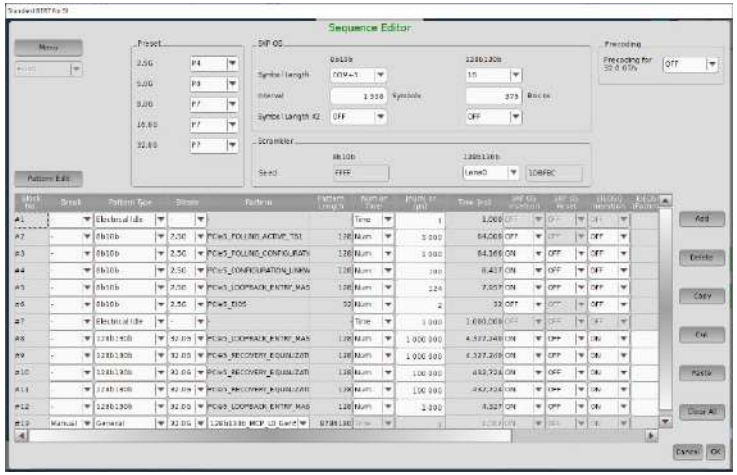
# Link Problem Test using Built-in Sequence Editor Function

The PCI-Express and USB 3.2 tests require evaluation by BER measurement when negotiation with the Link partner is completed. If this negotiation is not completed, although it is possible to use the LTSSM analysis function to troubleshoot the problem state, the built-in Sequence Editor function can troubleshoot the problem using detailed cause analysis. This function can be used to resolve negotiation problems quickly.

Identifying Link non-negotiation state using LTSSM function




Identifying problem parameters using status data occurrence times, sequence and encode data editing




Sequence Editor Function
(MU195020A-050): PCIe 1/2/3/4, USB 3.2 Gen1/2
Sequence Editor Function PCIe 5 Extension
(MU195020A-051): PCIe 5 Extension

# New Features of MP1900A Series

- 8-slot Platform
- 32G SI PPG/ED and Noise Generator Modules
- PCI Express Link Training and LTSSM Analysis Functions
- Backward Compatibility with SQA Series MU181000B Synthesizer, Jitter Modulation Source MU181500B, and 32G PPG/ED MU183020A/40B

Signal Quality Analyzer-R MP1900A

MX183000A-PL021 PCIe
MX183000A-PL025 PCIe Gen5 extension
MX183000A-PL022 USB
MX183000A-PL023 USB x2
Link Training (software)

21G/32G bit/s SI PPG MU195020A

21G/32G bit/s SI ED MU195040A

Noise Generator MU195050A

# 21G/32G bit/s SI PPG MU195020A Features

- Bit rate of 2.4 to 21 Gbit/s or 32.1 Gbit/s
- 1ch/2ch Selection
- 10Tap Emphasis built-in
- Data Output Amplitude 0.1 Vp-p to 1.3 Vp-p (Single-end)
  0.2 Vp-p to 2.6 Vp-p (Differential)
- Low Intrinsic Jitter output of 115 fs rms (typ.)
- Tr/Tf (20%-80%) of 12 ps (typ.)
- Multi-channel synchronization function
- NRZ/PAM4 support (PAM4 uses 2ch Data out + G0375A remote head)
- PCI Express / USB Link Training

**21G/32G bit/s SI PPG MU195020A**


Data1 (differential )  Data2 (differential)

・10Tap Emphasis
・High-Quality Output Waveforms
・Multi-channel Synchronization

DUT

# MU195020A PPG Data Output Waveforms

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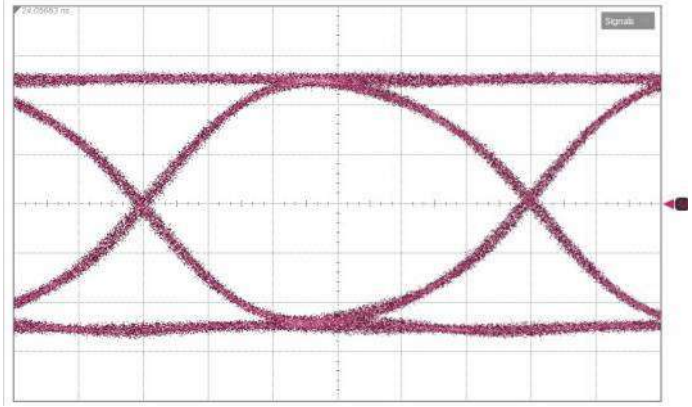
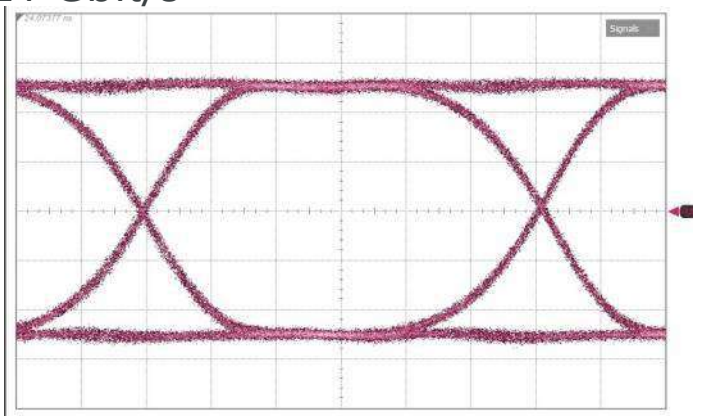
## Low Intrinsic Jitter Data Output Waveforms for Signal Integrity Analysis

PRBS $2^{31}$-1, 1 Vp-p (Single end, 70 GHz observed with oscilloscope)

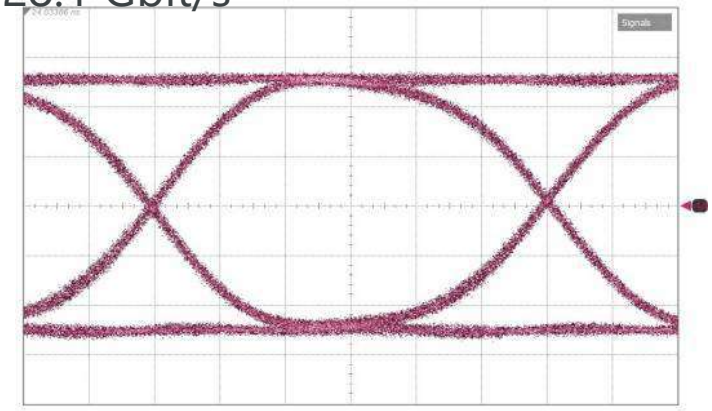
32.1 Gbit/s



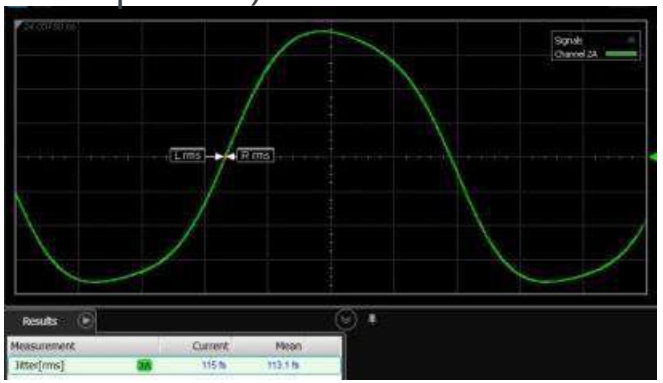
21 Gbit/s



28.1 Gbit/s



Low Intrinsic Jitter 115 fs (rms) @ 28.1 Gbit/s ("1010…" pattern)



# MU195020A PPG Data Output 10Tap Emphasis

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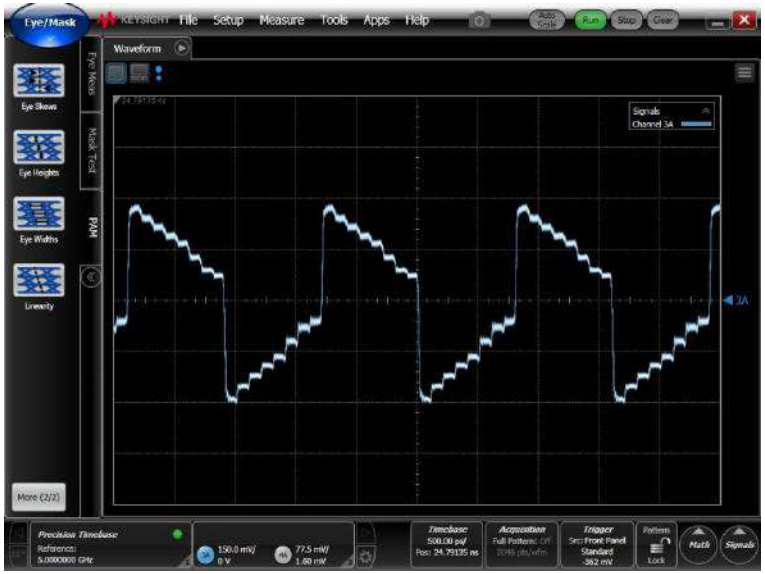
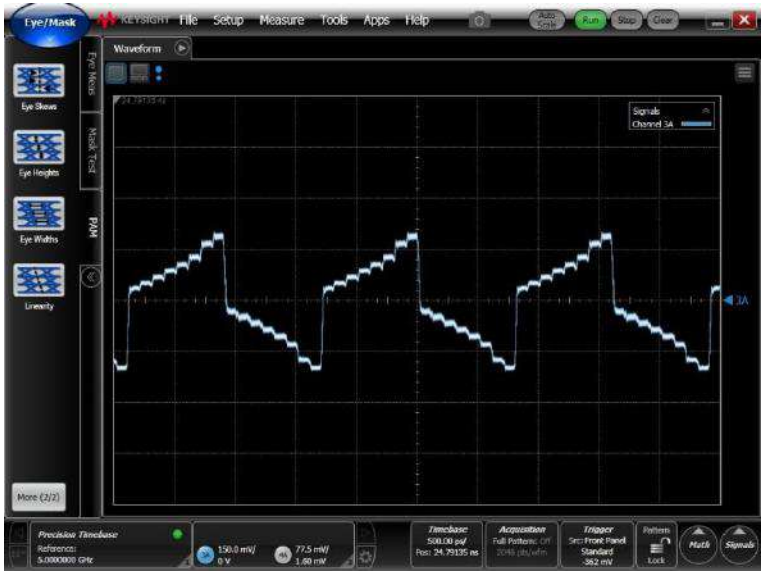
## Flexible Support for High-speed Device with Long-channel Design Evaluations

- 10Tap Emphasis
- Control up to 20 dB
- Pre-Emphasis output with peak output amplitude of 1.5 Vp-p




Waveform for correcting transmission path loss




Waveform emulating signal loss

Voltage control at each 1 bit for 10-bit time period

# MU195020A Data Output　Variable ISI

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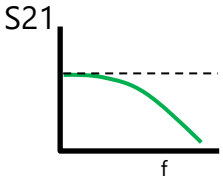
## Shorter Development Period by Eliminating Need for Multiple Test PC Boards

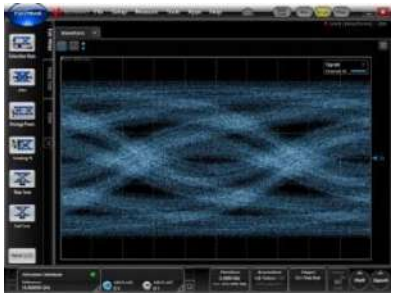
## Simple and High-Reproducibility Design Tests of High-Speed Device Channel Loss Dependency

- Emulate channel loss by controlling Emphasis and generate loss-compensated signals
- Automatically calculate Emphasis setting using S-parameter

MP1900A SQA-R




Emulate channel loss
And generate loss-compensated signals (Variable ISI option)



CEI-28G, 14 dB loss typical waveform (ISI function)


・**Manual Setting:**
Correct signal for target Eye Height/Width using 10Tap Emphasis function
・**Channel Emulator:**
Emulate S2P and S4P data loss insertion, and perform Emphasis compensation
・**ISI:**
Emulate ISI using CEI-28G/25G Nyquist frequency loss setting

# MU195020A PPG Multi-channel

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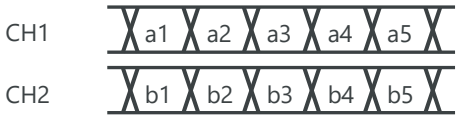
Multiplexing, high-bit-rate and crosstalk tests are supported by the multi-channel Data output, pattern synchronization and skew control functions for easy flexible evaluations of future high-bit-rate and multi-channel interfaces.

| Sync Channel Number | Supported Function | Application | Equipment Configuration |
|---|---|---|---|
| 2ch | 2ch Combination | 32G PAM4 Generation<br>2:1 MUX Evaluation | MU195020A 2ch PPG x1 |
| | Channel Synchronization | | |
| 4ch | 64G x 2ch Combination | 64G PAM4 Generation<br>4:1 MUX Evaluation | MU195020A 2ch PPG x2 |
| | Channel Synchronization | QSFP28 Evaluation | |

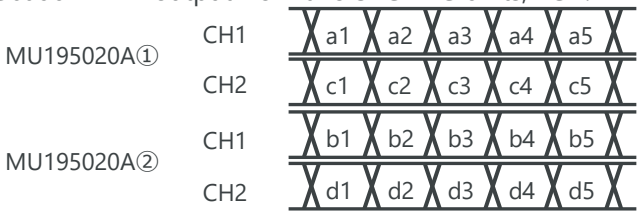
## ・2ch Combination

Supports shift to “a1b1 a2b2 . . .” pattern and PAM4 output.




## ・64G x 2ch Combination

Supports shift to “a1b1c1d1 a2b2c2d2 . . .” pattern and 64 Gbaud PAM4 output from two 32G PPG units, 4CH.




## ・Channel Synchronization

One 16ch MP1900A supports parallel interface evaluations, crosstalk tests and D/A converter evaluations as well as synchronized output for up to four MP1900A units.

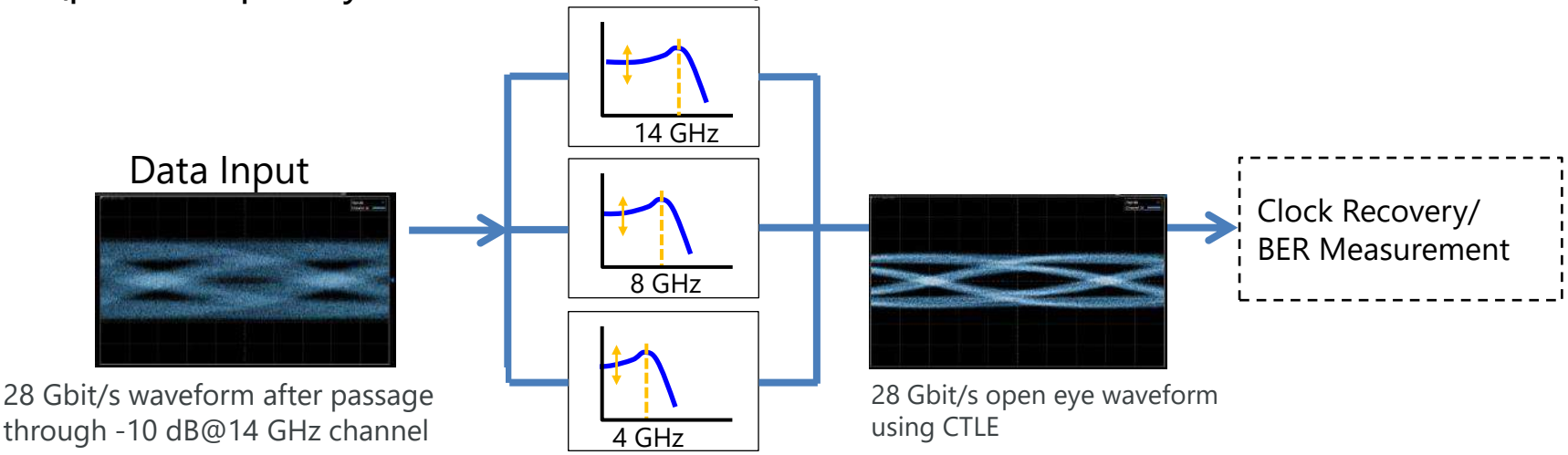
# 21G/32G bit/s SI ED MU195040A Features

- Bit rate of 2.4 to 21 Gbit/s or 32.1 Gbit/s
- 1ch/2ch selection
- Built-in multi-band CTLE function
  - Peak frequency: 14, 8, 4 GHz switchable
  - Gain control: 0 to –12 dB control
- Data input amplitude: 0.05 to 1.0 Vp-p (Single-end)
- Input sensitivity @ 28.1Gbit/s NRZ: 15 mV (Eye Height) (typ.); 22 mVp-p (Eye amplitude)
  @ 28.1Gbit/s PAM4: 30 mV/Eye(Eye Height) (typ.); 150 mVp-p (Eye amplitude)
- Auto-measurements (Auto-search/Adjust, Eye Contour, Bathtub, Jitter Tolerance)
- Clock Recovery: 2.4  to 32.1 Gbit/s, SSC support
- PCI Express / USB Link Training

**MU195040A　21G/32G bit/s SI ED**

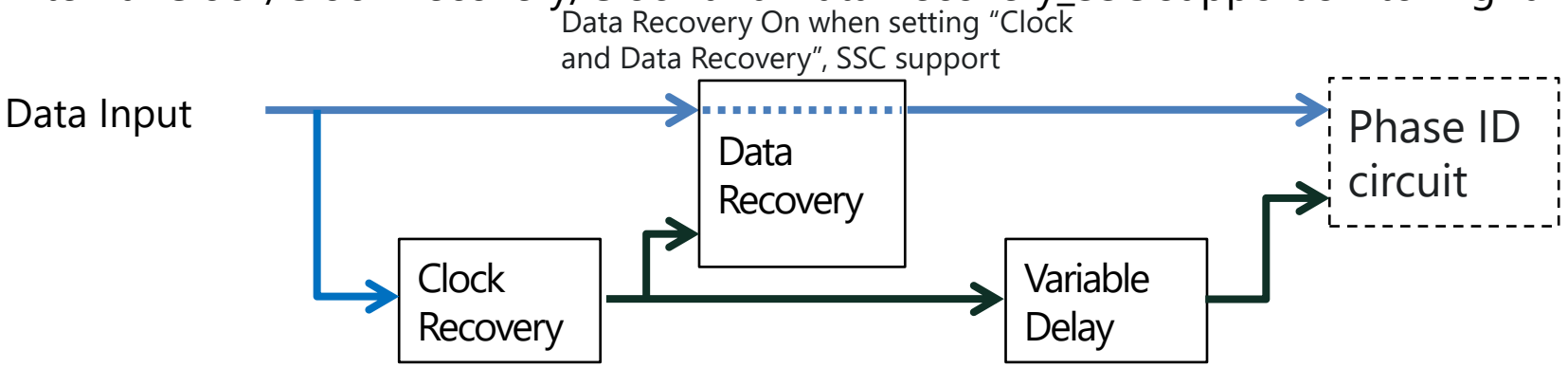
# MU195040A ED Data Input CTLE/Clock Recovery Functions

Supports input receiver measurements for CEI-28G, PCIe Gen 3 to Gen 5 using 3-band CTLE (peak frequency of 14, 8 , and 4 GHz)




Supports SSC to implement Eye analysis for input signals with added Jitter

- 2.4 Gbit/s to 32.1 Gbit/s (extracts Clock from Data1 input signal)
- External Clock/Clock Recovery/Clock and Data Recovery_SSC support switching function



# MU195040A ED Auto Measurement・Analysis Functions

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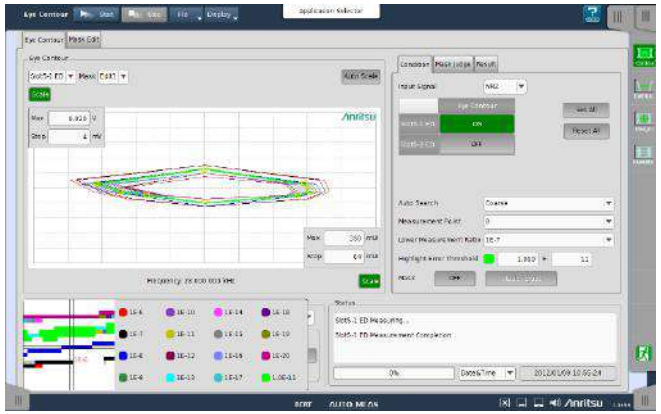
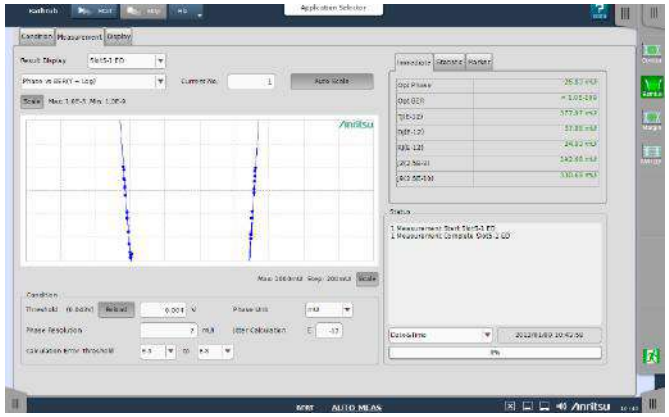
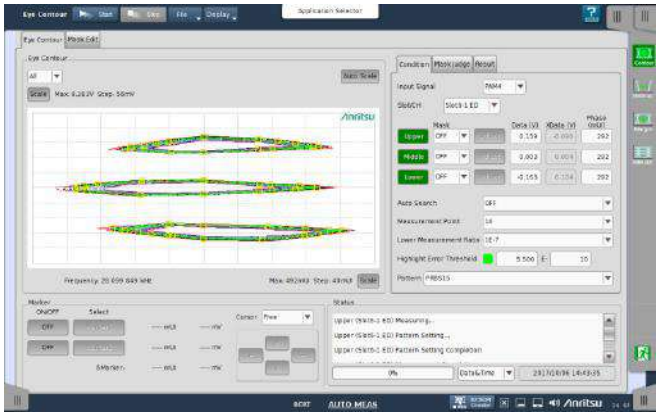
Higher-accuracy Eye analysis is supported using the auto-measurement and auto-analysis functions, such as Auto Search/Auto Adjust, Bathtub, Eye Contour, Eye Margin, and PAM BER measurement that make use of the measurement high-input-sensitivity performance.



Example of Eye Contour Measurement at Input of Small 50 mVp-p Signal



Bathtub Measurement Example



Example of Eye Contour Measurement at Input of PAM4 Signal

# Noise Generator MU195050A Features

Supports Voltage Noise Tolerance tests specified by CEI and IEEE802.3 for backplane, PCIe, and Thunderbolt measurements

- Noise addition to Data signals up to bit rates of 32.1 Gbit/s
- 2ch output
- CMI/DMI/White noise support
  - Common mode noise frequency: 0.1 GHz to 6 GHz
  - Differential mode noise frequency: 2 GHz to 10 GHz
  - White noise band: 10 GHz; Crest Factor: >5
- Supports external noise input

MU195020A

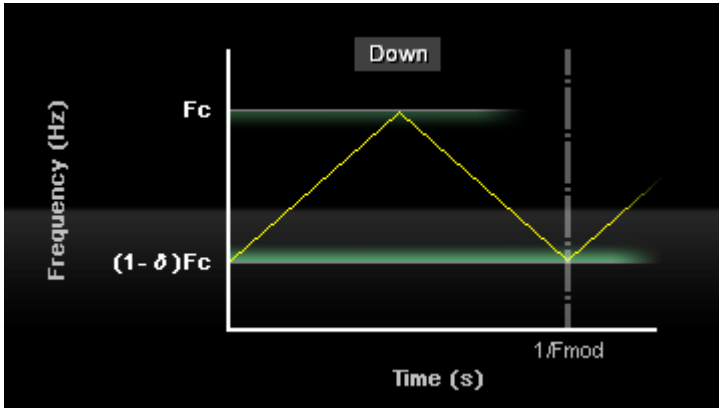
**MU195050A**
**Noise Generator**


- **Built-in CMI/DMI/White noise**
- **2ch output**

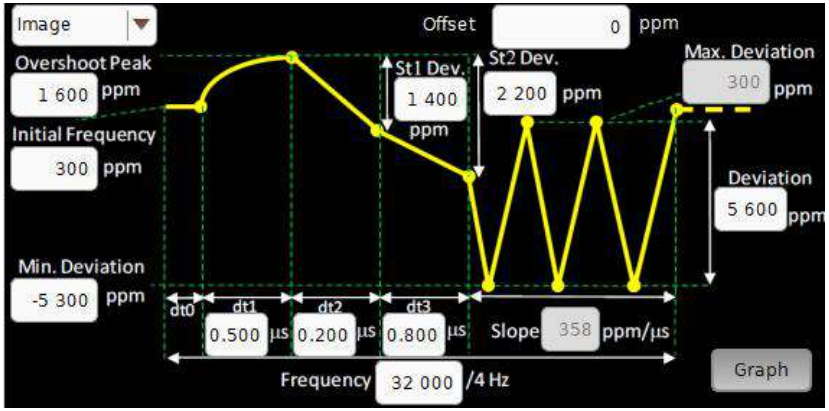
DUT

# MU181500B Jitter SSC Profile Function

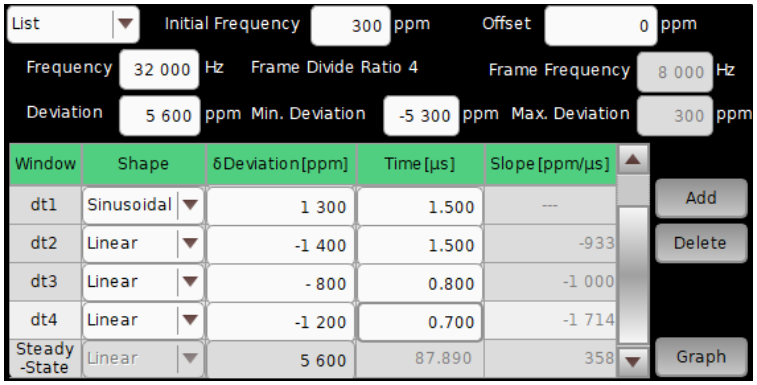
The new SSC Profile standard for USB 4, Display Port, etc., makes it easy to test SSC compliance of the DUT receiver clock recovery, etc.



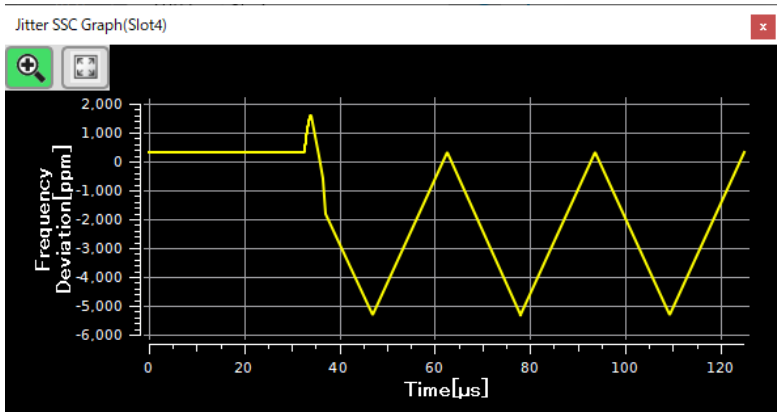

Previous Triangular




USB 4 SSC Profile (image)

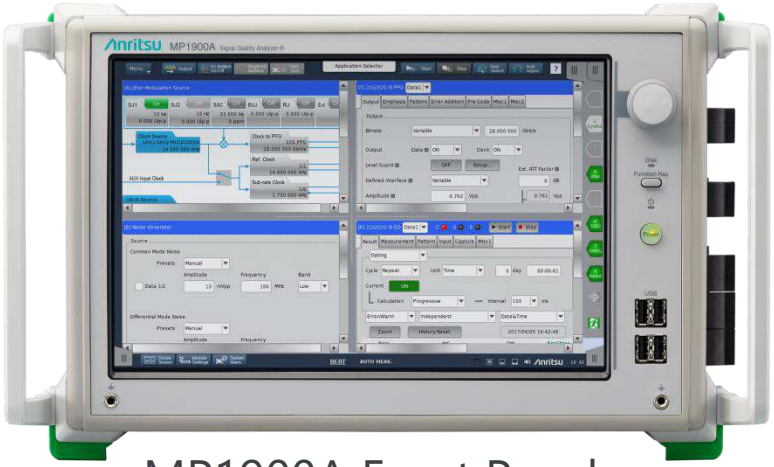



Variable Profile (List)




Variable Profile (Graph)

# MP1900A Main Unit Features



MP1900A Front Panel

- 8 Slots
- Install up to eight 2ch PPG and ED modules
- Synchronize up to four MP1900A main units
  → Expansion to 2 Tbit/s
- Backwards compatibility with existing MP1800A modules

MP1900A Side Panel

- Touch Screen
- GPIB x 1, and Ethernet x 2
- USB x 6, HDMI x 1, and D-SUB x 1
- Windows 10 IoT Enterprise

# MP1900A 8-slot Main Unit Expandability

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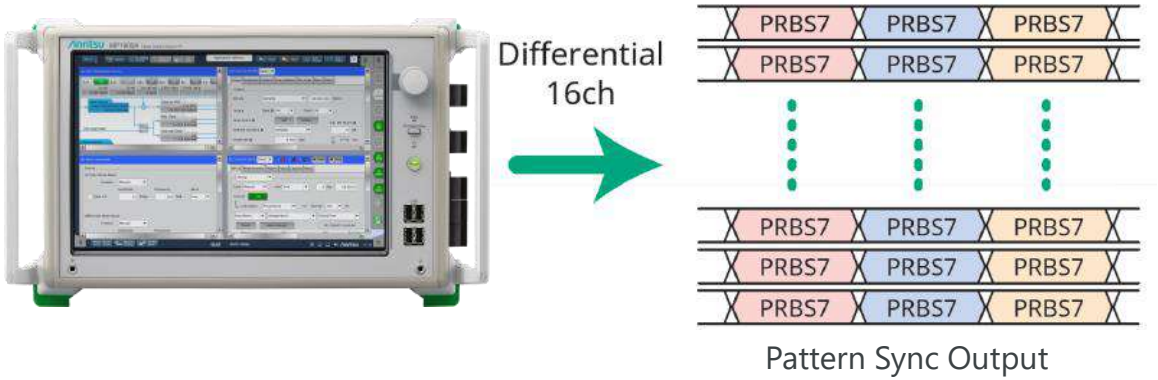
## Future-proof Main Unit Expandability

- One Main Unit Supports 16ch Transmissions for Future High Bit Rates




- Multi-channel Synchronized Output of Four MP1900A Main Units

# System View User Interface and Improved Operability using Multiple Windows

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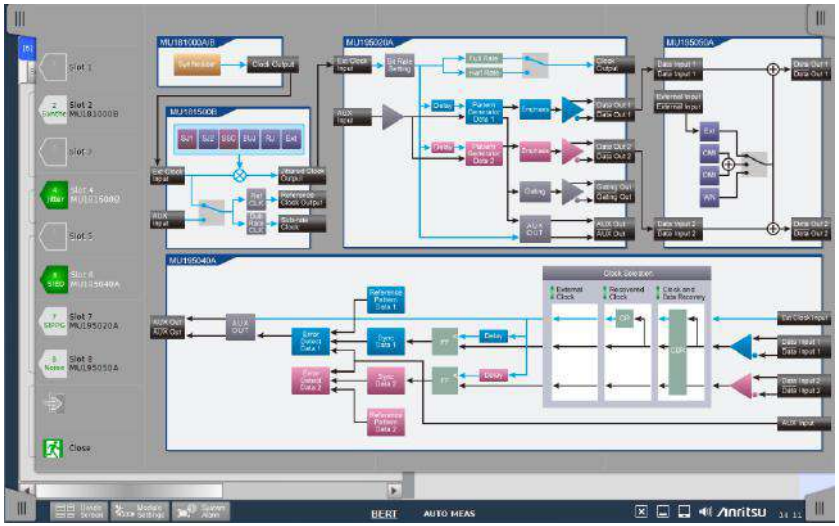
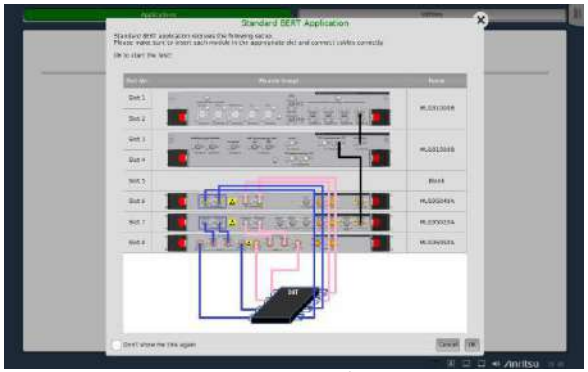
Advancing beyond

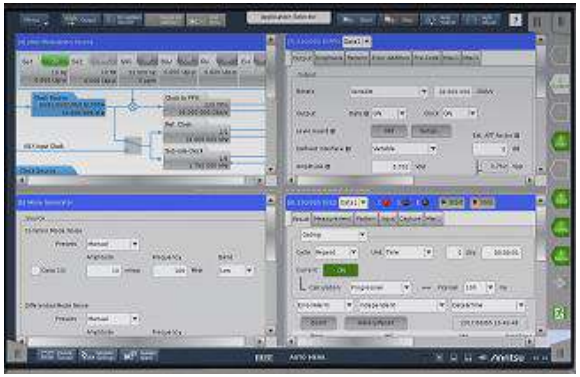
Operability is improved by the large 12.1-inch LCD touch panel and intuitive GUI. The newly developed System View user interface displays easy-to-understand system function blocks with help guidance for system settings and easy operation of each module.



System View User Interface



Setup Instructions



4ch Multi-channel Measurement Results on One Screen

# EZ SCPI Creator

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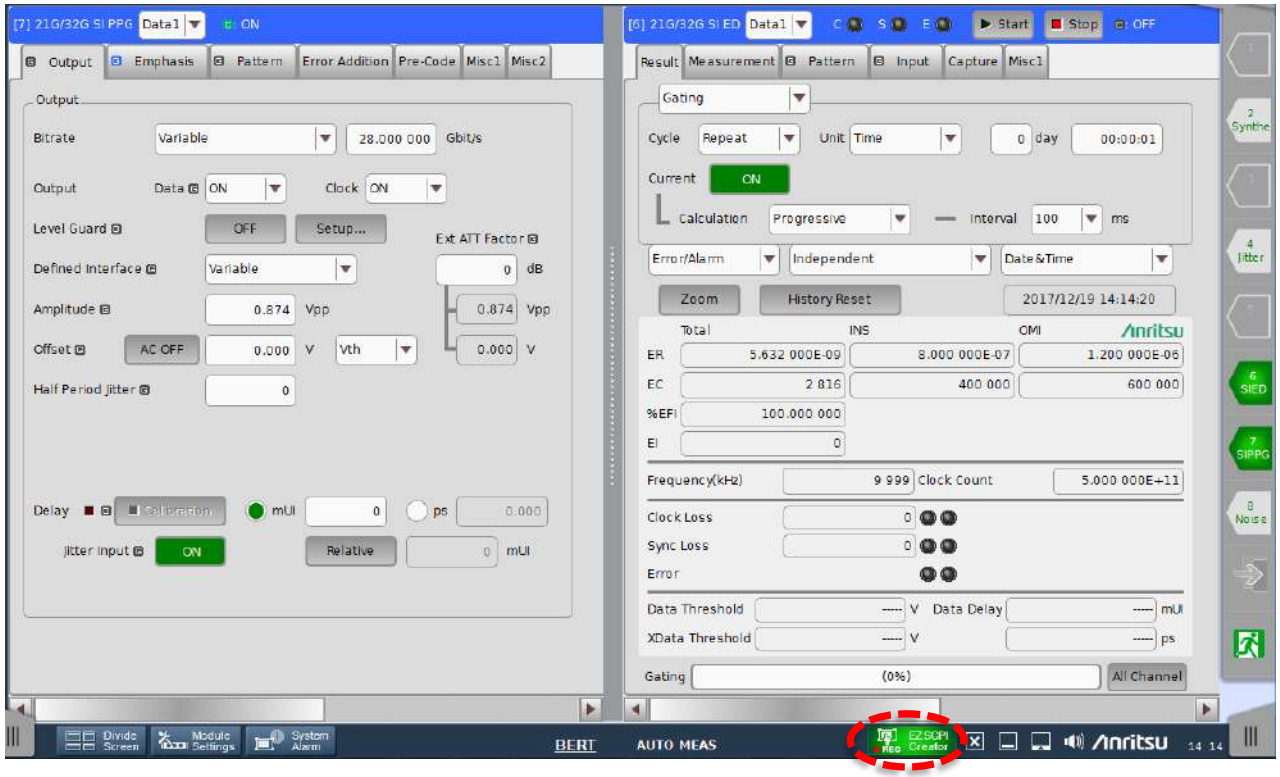
Advancing beyond

Operation while EZ SCPI Creator is ON creates remote command strings automatically, making it easy to describe remote commands.




## EZ SCPI Creator ON

For example, executing the following operations:

- Set PPG Amplitude
- Set PPG Pattern Type
- Set PPG PRBS Length
- Set Output On
- Start ED measurement

Automatically generates these operation remote commands

```
:UENTry:ID 1; :MODule:ID 7; :INTerface:ID 1; :OUTPut:DATA:AMPLitude DATA,0.574
:UENTry:ID 1; :MODule:ID 7; :INTerface:ID 1; :SOURce:PATTern:TYPE PRBS
:UENTry:ID 1; :MODule:ID 7; :INTerface:ID 1; :SOURce:PATTern:PRBS:LENG 31
:SOURce:OUTPut:ASET ON
:UENTry:ID 1; :MODule:ID 6; :INTerface:ID 1; :SENSe:MEASure:STAR
```

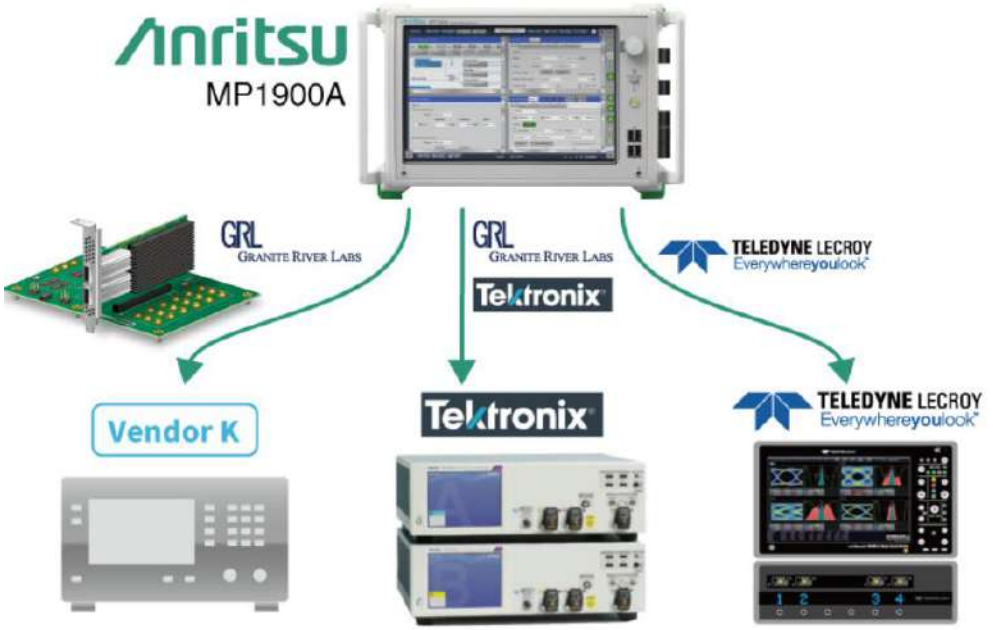
# PCI Express Test Solution

# PCIe Tx LEQ/Rx Compliance Test

- Combination of best-performance BERT MP1900A and preferred oscilloscope -

## Shorter test times and reduced investment cost

- Supports Combination with Lecroy/Tektronix/Keysight Real-Time Oscilloscopes
- Automated Rx CEM and Base Tests: Calibration, Link EQ and Automated Tx Test
- Protocol Aware: Link Training/Equalization and LTSSM Analysis
- High-Expandability 32G Multichannel BERT for PCIe1 to 5




Best BERT Performance

Fully Automated SW and Analysis

Preferred Oscilloscope

# MP1900A Series PCI Express Test Solution

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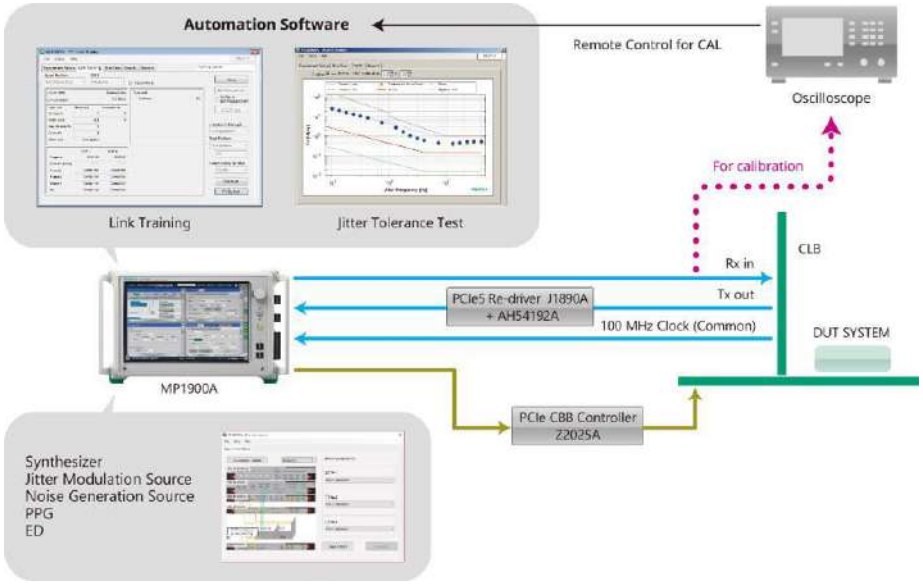
| Measurement Item | Supported Software |
|---|---|
| Transmitter Test | * |
| Tx Response Time | MX183000A-PL021<br>PL025 (Gen5) |
| Stressed Signal Calibration | * |
| Transition to Loopback State | MX183000A-PL021<br>PL025 (Gen5) |
| Rx Link Equalization Test | MX183000A-PL021 |
| Jitter Tolerance Test | MX183000A-PL001 |
| PLL Loop Bandwidth Test | * |

*Contact your sales representative about expected future support.

# MP1900A Series PCI Express Receiver Test Solution

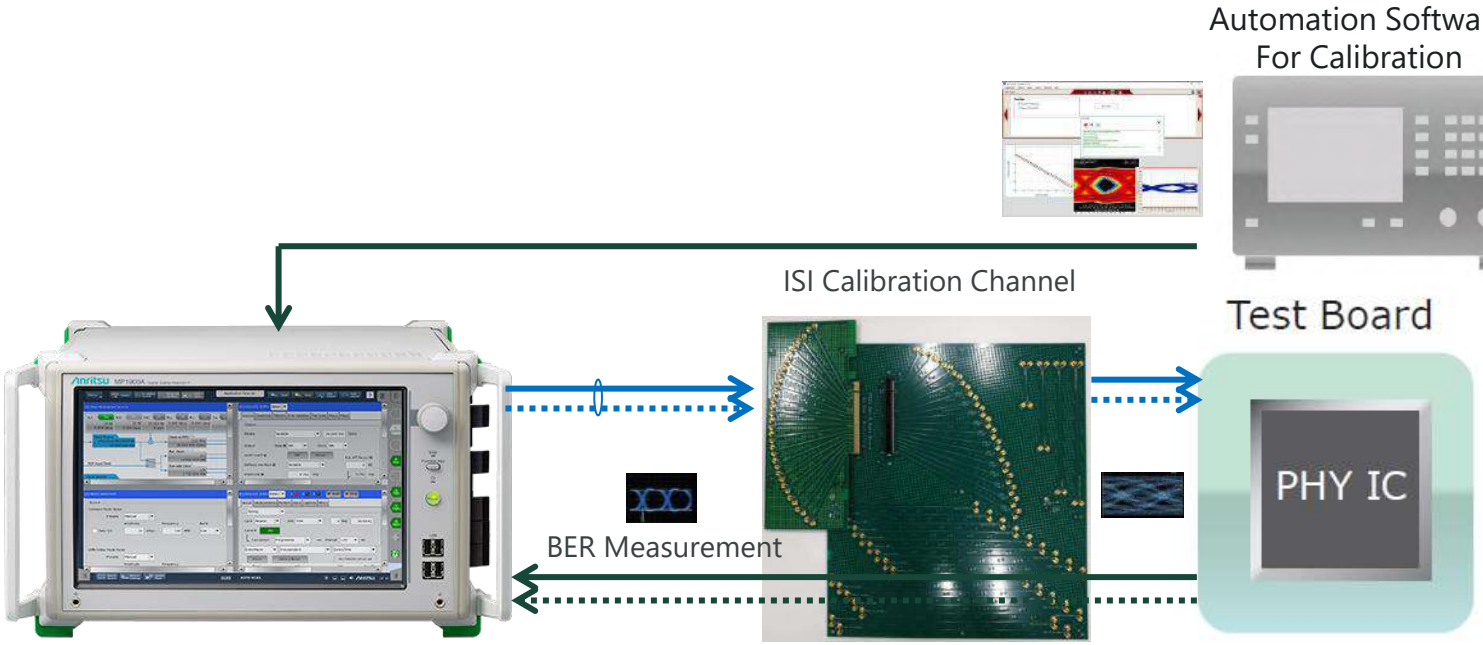
- All-in-one PCI Express Gen1 to 5 solution
- Wideband bit rate of 2.4 Gbit/s to 21 Gbit/s, expansion to 32.1 Gbit/s
  No need for hardware upgrade to support Gen5 (32 GT/s)
- Automated LEQ test (Protocol Aware) with LTSSM event trigger function
- Low-Jitter test signals and high-input sensitivity performance
- Link Training and LTSSM analysis function
- SKP Order set and 8B/10B, 128B/130B coding
- Built-in noise (CMI and DMI) and Jitter (SJ, RJ, BUJ and SSC) addition function
- Supports both Common (MU181000B-002) and Separate Clock architectures
- Establishes Gen5 return path using external Re-Driver set



# PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (1/5)

## PCI Express PHY IP Device Rx Test Sequence

| Stress Signal Calibration | Transition to Loopback Status | Stress Signal Input Test |
|---|---|---|
| Applicable Software | | |
| Automation Software:<br>GRL-PCIE5-BASE/CEM-RXA<br>or QPHY-PCIE-Tx-Rx | Link Training Software:<br>MX183000A-PL021 (Gen1 to 4)<br>MX183000A-PL025 (Gen5) | ・Jitter Tolerance Margin Test:<br>MX183000A-PL001<br>or<br>・Jitter Sweep Test (Pass/Fail):<br>GRL-PCIE5-BASE/CEM-RXA<br>or QPHY-PCIE-Tx-Rx |



# PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (2/5)

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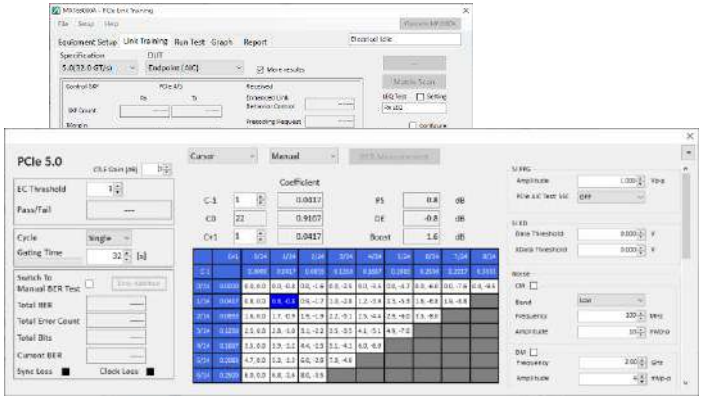
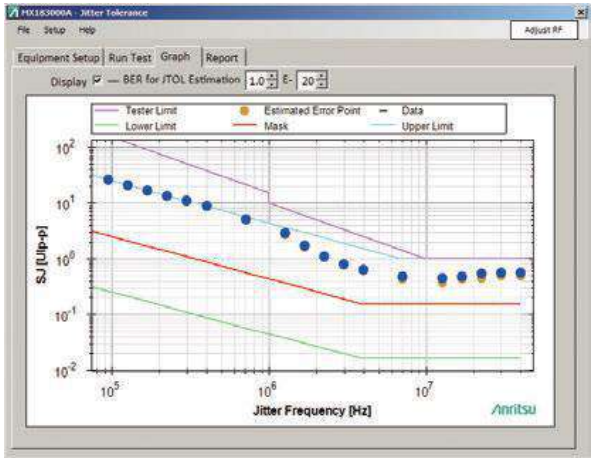
Combining the PCIe Link Training MX183000A-PL021 and Jitter Tolerance Test MX183000A-PL001 software supports tests from the Link with the DUT to the Jitter Tolerance test measurements required by PCI Express receiver tests.

Displays Link Training Settings and Results




Automatic Measurement of Receiver Jitter Tolerance




| Item | MX183000A-PL021 Specifications | PL025 Extension |
|---|---|---|
| Standard | PCI Express Rev 1.x (2.5 GT/s), 2.0 (5 GT/s), 3.x (8 GT/s), 4.0 (16 GT/s) | Gen5 (32 GT/s) |
| Test Pattern | Compliance (MCP, CP), PRBS (7, 9, 10, 11, 15, 20, 23, 31) | |
| LTSSM State | Transition to Detect, Polling, Configuration, Recovery, Loopback | |
| Loopback Through | Configuration, Recovery | |
| TS Setting Parameters | SKP Insertion, 8B/10B, 128B/130B, FTS, Link Number, Lane Number, Scrambling | |

# PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (3/5)

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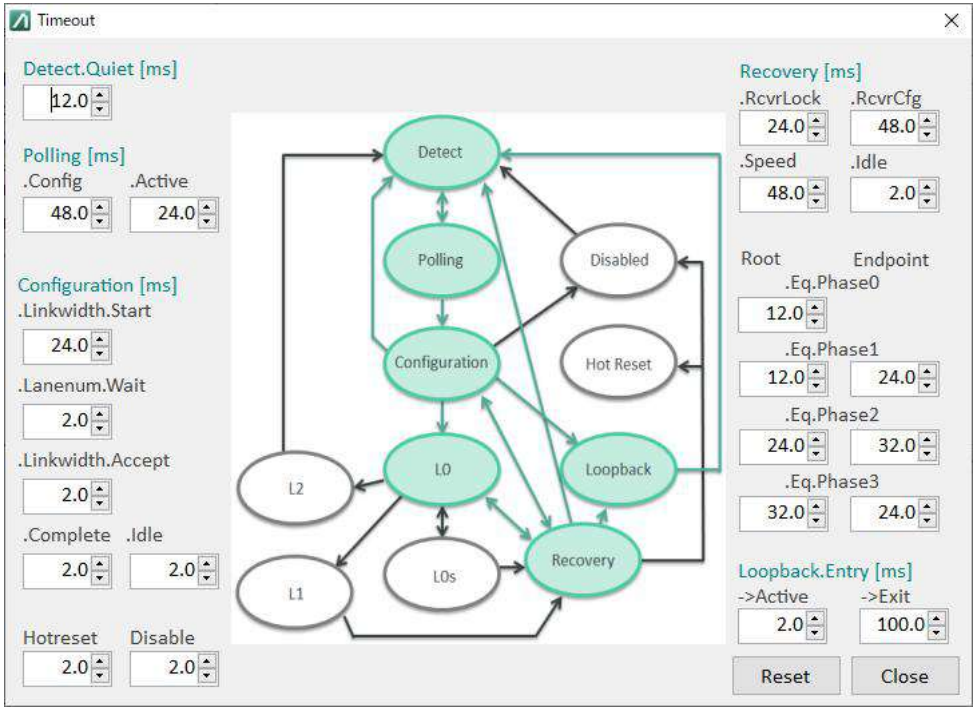
## Shorter Development Period by LTSSM Analysis Functions for Troubleshooting Cause of Link Faults

Examine each state transition time and path from "Detect" to "Loopback".




Check results for each state transition using Training Log Viewer.

Training Log Viewer

| Time [ns] | ΔTime [ns] | State | Speed[GT/s] | Detect Preset |
|---|---|---|---|---|
| 440,750,376 | 4 | RECOVERY_RCVR_LOCK | 16.0 | ---- |
| 440,750,380 | 1,153,864 | RECOVERY_EQUALIZATION_PHASE0 | 16.0 | ---- |
| 441,904,244 | 8 | RECOVERY_EQUALIZATION_PHASE0 | 16.0 | ---- |
| 441,904,252 | 2,848 | RECOVERY_EQUALIZATION_PHASE1 | 16.0 | ---- |
| 441,907,100 | 272 | RECOVERY_EQUALIZATION_PHASE2 | 16.0 | 0 (MP1900A ==> DUT) |
| 441,907,372 | 1,999,728 | RECOVERY_EQUALIZATION_PHASE2 | 16.0 | 1 (MP1900A <== DUT) |
| 443,907,100 | 2,864 | RECOVERY_EQUALIZATION_PHASE2 | 16.0 | 0 (MP1900A ==> DUT) |
| 443,909,964 | 2,000,000 | RECOVERY_EQUALIZATION_PHASE2 | 16.0 | 1 (MP1900A <== DUT) |
| 445,909,964 | 2,860 | RECOVERY_EQUALIZATION_PHASE3 | 16.0 | 0 (MP1900A ==> DUT) |
| 445,912,824 | 4 | RECOVERY_EQUALIZATION_PHASE3 | 16.0 | 1 (MP1900A <== DUT) |
| 445,912,828 | 1,999,980 | RECOVERY_EQUALIZATION_PHASE3 | 16.0 | 0 (MP1900A ==> DUT) |
| 447,912,808 | 4 | RECOVERY_EQUALIZATION_PHASE3 | 16.0 | 1 (MP1900A <== DUT) |
| 447,912,812 | 2,002,840 | RECOVERY_EQUALIZATION_PHASE3 | 16.0 | 0 (MP1900A ==> DUT) |
| 449,915,652 | 64 | RECOVERY_RCVR_LOCK | 16.0 | ---- |
| 449,915,716 | 2,980 | RECOVERY_RCVR_CFG_TS2 | 16.0 | ---- |
| 449,918,696 | 508 | RECOVERY_IDLE | 16.0 | ---- |
| 449,919,204 | 12 | L0 | 16.0 | ---- |
| 449,919,216 | 2,420 | RECOVERY_RCVR_LOCK | 16.0 | ---- |
| 449,921,636 | 6,553,832 | RECOVERY_RCVR_CFG_EQTS2 | 16.0 | ---- |
| 456,475,468 | 100,016 | RECOVERY_SPEED | 16.0 | ---- |
| 456,575,484 | 32 | RECOVERY_SPEED | 32.0 | ---- |
| 456,575,516 | 4 | RECOVERY_RCVR_LOCK | 32.0 | ---- |
| 456,575,520 | 1,213,648 | RECOVERY_EQUALIZATION_PHASE0 | 32.0 | ---- |
| 457,789,168 | 8 | RECOVERY_EQUALIZATION_PHASE0 | 32.0 | ---- |
| 457,789,176 | 1,892 | RECOVERY_EQUALIZATION_PHASE1 | 32.0 | ---- |
| 457,791,068 | 264 | RECOVERY_EQUALIZATION_PHASE2 | 32.0 | 0 (MP1900A ==> DUT) |
| 457,791,332 | 1,999,736 | RECOVERY_EQUALIZATION_PHASE2 | 32.0 | 1 (MP1900A <== DUT) |
| 459,791,068 | 1,912 | RECOVERY_EQUALIZATION_PHASE2 | 32.0 | 0 (MP1900A ==> DUT) |
| 459,792,980 | 2,000,000 | RECOVERY_EQUALIZATION_PHASE2 | 32.0 | 1 (MP1900A <== DUT) |
| 461,792,980 | 1,912 | RECOVERY_EQUALIZATION_PHASE3 | 32.0 | 0 (MP1900A ==> DUT) |
| 461,794,892 | 4 | RECOVERY_EQUALIZATION_PHASE3 | 32.0 | 1 (MP1900A <== DUT) |
| 461,794,896 | 2,000,004 | RECOVERY_EQUALIZATION_PHASE3 | 32.0 | 0 (MP1900A ==> DUT) |
| 463,794,900 | 4 | RECOVERY_EQUALIZATION_PHASE3 | 32.0 | 1 (MP1900A <== DUT) |
| 463,794,904 | 2,001,908 | RECOVERY_EQUALIZATION_PHASE3 | 32.0 | 0 (MP1900A ==> DUT) |
| 465,796,812 | 32 | RECOVERY_RCVR_LOCK | 32.0 | ---- |
| 465,796,844 | 1,948 | RECOVERY_RCVR_CFG_TS2 | 32.0 | ---- |
| 465,798,792 | 524 | LOOPBACK_ENTRY_MASTER_TS1 | 32.0 | ---- |
| 465,799,316 | 0 | LOOPBACK_ACTIVE_MASTER | 32.0 | ---- |

# PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (4/5)

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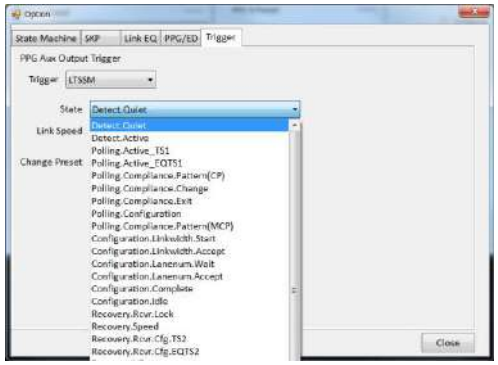
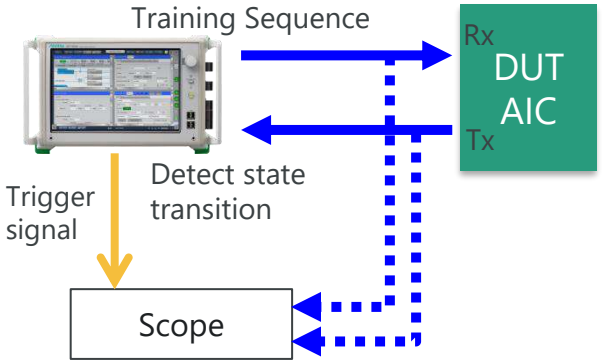
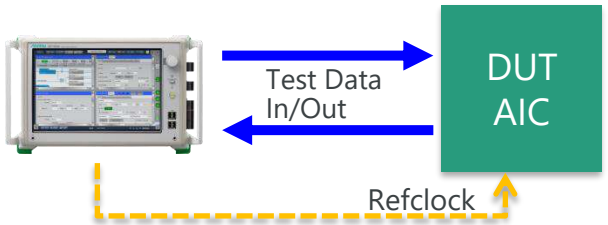
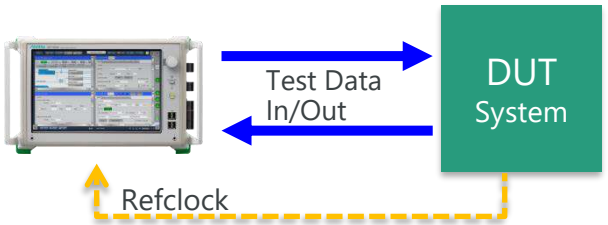
Generate trigger at LTSSM transition timing to support examination using oscilloscope waveform.




Supports both common and separate Refclock test architectures and SRIS



# PCI Express Link Training, LTSSM Analysis and Jitter Tolerance Measurements (5/5)

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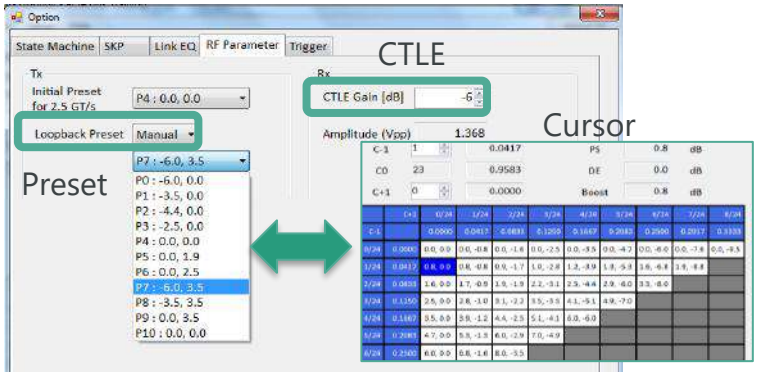
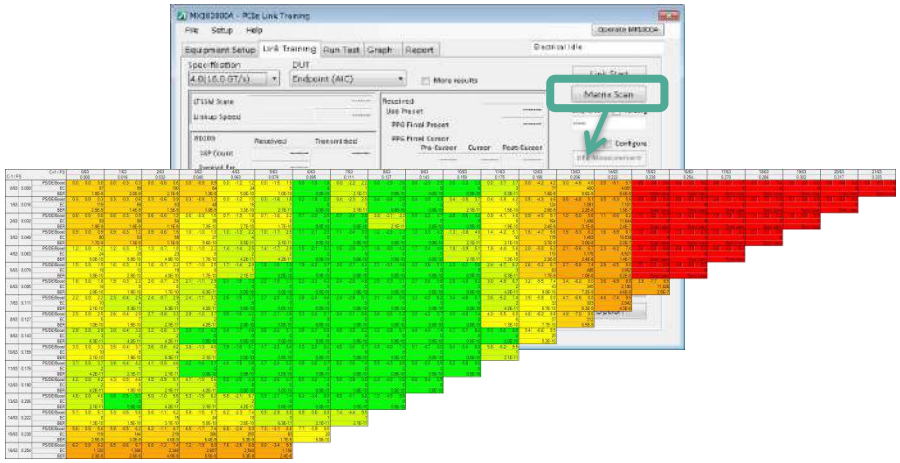
Advancing beyond

## Matrix Scan Function

To secure high-quality communications with the Link partner, the best combination of the Tx-side EQ and Rx-side EQ must be selected.
The Matrix scan function scans for the best Tx EQ setting at the receiver
to find the best setting automatically at the receiver




Graphical display of BER measurement results for each DUT Tx Preset setting

# PCI Express Receiver Test Recommended Equipment List (1/2)

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MP1900A | Signal Quality Analyzer-R | - | 1 | |
| MU181000B | 12.5GHz 4port Synthesizer | 002 | 1 | |
| MU181500B | Jitter Modulation Source | - | 1 | |
| MU195020A | 21G/32G bit/s SI PPG | 001*, 010, 011 | 1 | *Add Opt-001 for expansion to Gen5 (32 G) |
| MU195040A | 21G/32G bit/s SI ED | 001*, 010, 011, 022 | 1 | |
| MU195050A | Noise Generator | - | 1 | |
| MX183000A-PL001 | Jitter Tolerance Test | - | 1 | |
| MX183000A-PL021 | PCIe Link Training | - | 1 | Gen1-4 |
| MX183000A-PL025 | PCIe Gen5 Link Training Software | - | 1 | PL021 required to add PL025 |
| J1815A | MP1900A PCIe Measurement Component Set | - | 1 | |
| Z2025A | PCIe CBB Controller | - | 1 | for Add-in-card tests, supports GRL automation software |
| Z2029A | PCIe 100 MHz Reference Clock Buffer | - | 1 | for Add-in-card tests |
| J1890A + AH54192 | PCIe Re-Driver | - | 1 | Recommended when System test return path is 18 dB or more |

# PCI Express Receiver Test Recommended Equipment List (2/2)

Choose the automation software matching your oscilloscope.

| Model | Electrical Test | Remark |
|---|---|---|
| QPHY-PCIE-Tx-Rx | PCIE Gen3/4/5 Tx, Rx | Teledyne LeCroy scope<br>Purchase from Teledyne LeCroy |
| GRL-PCIE4-BASE-RXA | PCIE Gen4 Base Rx | Tektronix or Keysight scope<br>Purchase from Granite River Labs |
| GRL-PCIE4-CEM-RXA | PCIE Gen4 CEM Rx | |
| GRL-PCIE5-BASE-RXA | PCIE Gen5 Base Rx | |
| GRL-PCIE5-CEM-RXA | PCIE Gen5 CEM Rx | |

# Meeting Next-Generation Standards

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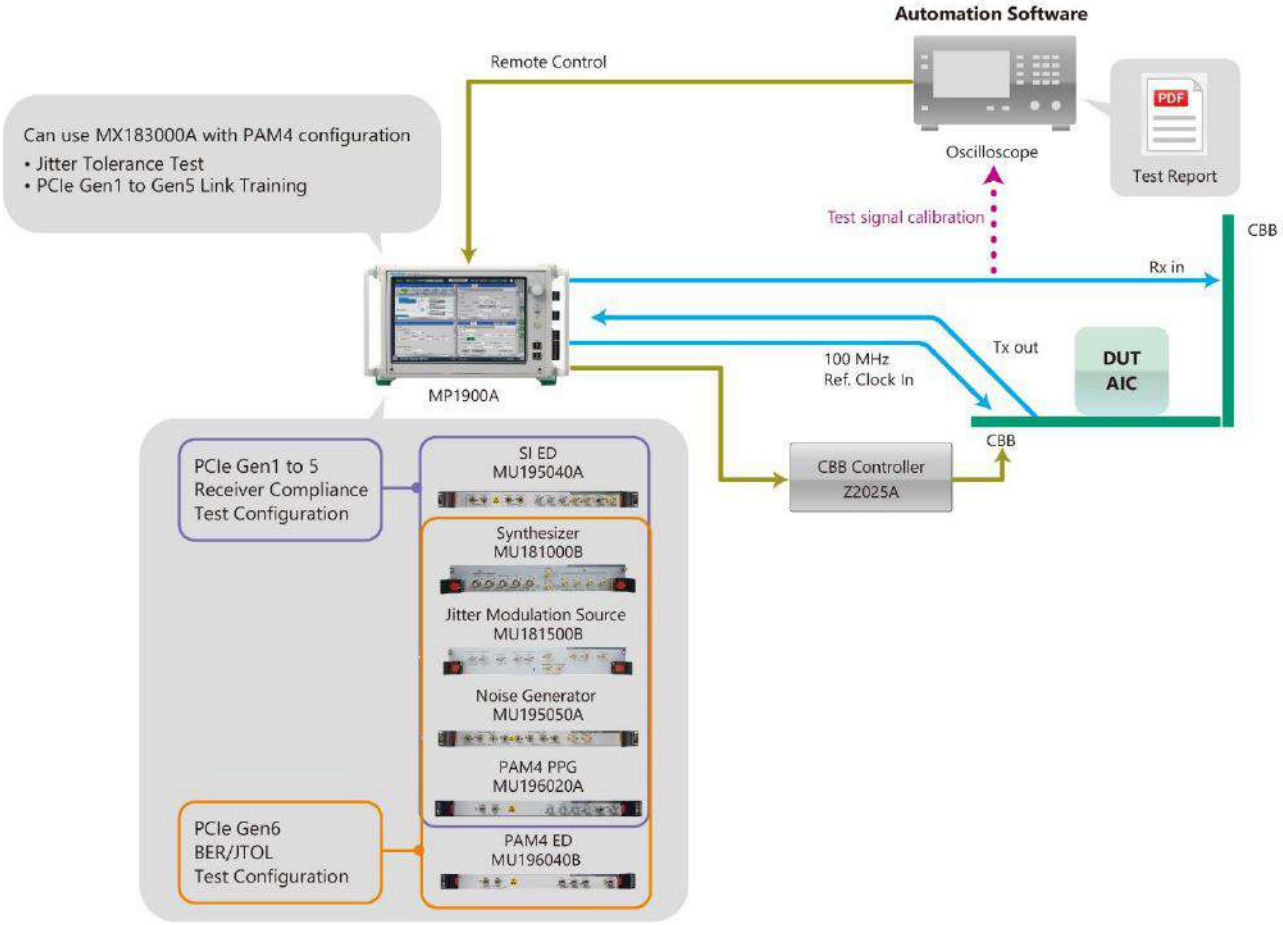
Next-generation PCIe Gen6 uses PAM4 interfaces. The all-in-one MP1900A with PAM4 PPG module covers PCIe Gen1 to Gen5 compliance tests including Link negotiation, Gen6 PAM4 BER measurements, and JTOL measurements, helping facilitate a smooth transition to PCIe Gen6.*




*Contact our business section about Gen6 compliance tests.

# PCIe Gen1 to 6 Receiver Test Recommended Equipment List (1/2)

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MP1900A | Signal Quality Analyzer-R | - | 1 | |
| MU181000B | 12.5GHz 4port Synthesizer | 002 | 1 | |
| MU181500B | Jitter Modulation Source | - | 1 | |
| MU196020A | PAM4 PPG | 001, 011 | 1 | Gen1-6*1 |
| MU195040A | 21G/32G bit/s SI ED | 001, 010, 011, 022 | 1 | Gen1-5*2 |
| MU196040B | PAM4 ED | 001, 011, 022, 041 | 1 | Gen6*2 |
| MU195050A | Noise Generator | - | 1 | |

*1: PAM4 PPG also supports PCIe Gen1 to Gen5 Link Negotiation and Compliance tests using the GRL automation software with the MX183000A.
*2: The MU195040A is required for PCIe Gen1 to Gen5 for Compliance test. The MU196040B supports PAM4 signal BER measurements along with Jitter Tolerance measurements.

# PCIe Gen1 to 6 Receiver Test Recommended Equipment List (2/2)

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MX183000A-PL001 | Jitter Tolerance Test | - | 1 | |
| MX183000A-PL021 | PCIe Link Training | - | 1 | Gen1-4 |
| MX183000A-PL025 | PCIe Gen5 Link Training Software | - | 1 | PL021 is required to add PL025 |
| J1815A | MP1900A PCIe Measurement Component Set | - | 1 | |
| Z2025A | PCIe CBB Controller | - | 1 | for Add-in-card tests, supports GRL automation software |
| Z2029A | PCIe 100 MHz Reference Clock Buffer | - | 1 | for Add-in-card tests |

Choose the automation software matching your oscilloscope.

| Model | Electrical Test | Remark |
|---|---|---|
| GRL-PCIE4-BASE-RXA | PCIE Gen4 Base Rx | Tektronix or Keysight scope<br>Purchase from Granite River Labs |
| GRL-PCIE4-CEM-RXA | PCIE Gen4 CEM Rx | |
| GRL-PCIE5-BASE-RXA | PCIE Gen5 Base Rx | |
| GRL-PCIE5-CEM-RXA | PCIE Gen5 CEM Rx | |

# USB Type-C Test Solution

# USB Type-C Receiver Test Solution

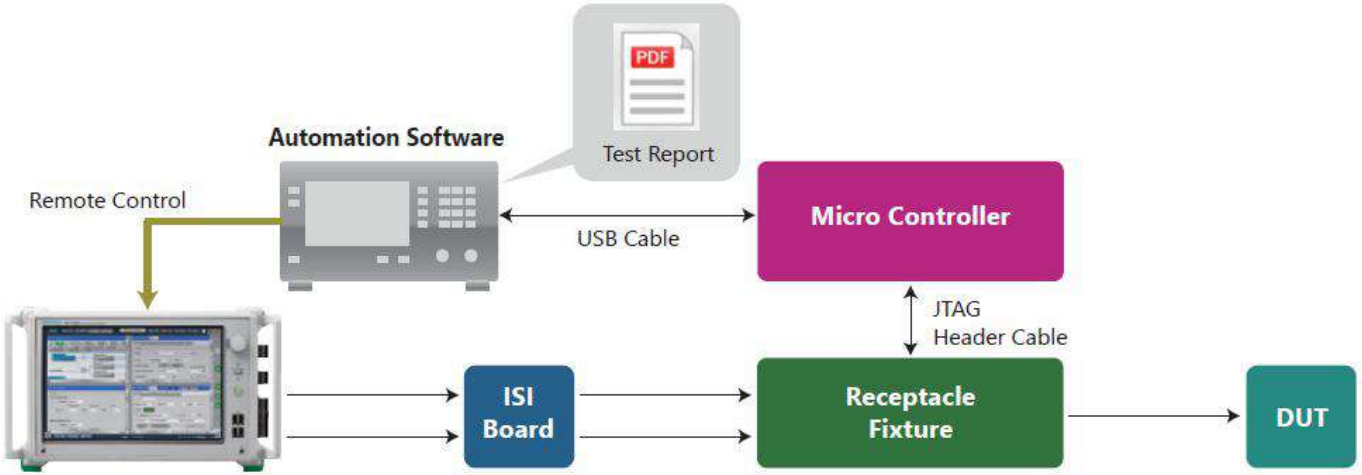
- Wideband operation from 2.4 Gbit/s to 21 Gbit/s with expansion to 32.1 Gbit/s without hardware upgrade.

  Same configuration supports receiver tests of USB Type-C interfaces (USB 3.2, USB4, Thunderbolt 3, DisplayPort 1.4) .
- Combination with automation software supports oscilloscope from main makers

  Simplifies complex test procedures and reduces work burden by using own oscilloscope
- High-performance multichannel BERT with high-quality output waveforms (12-ps Tr/Tf, 115-fs rms Intrinsic Jitter) and high-input sensitivity (15 mV EH)

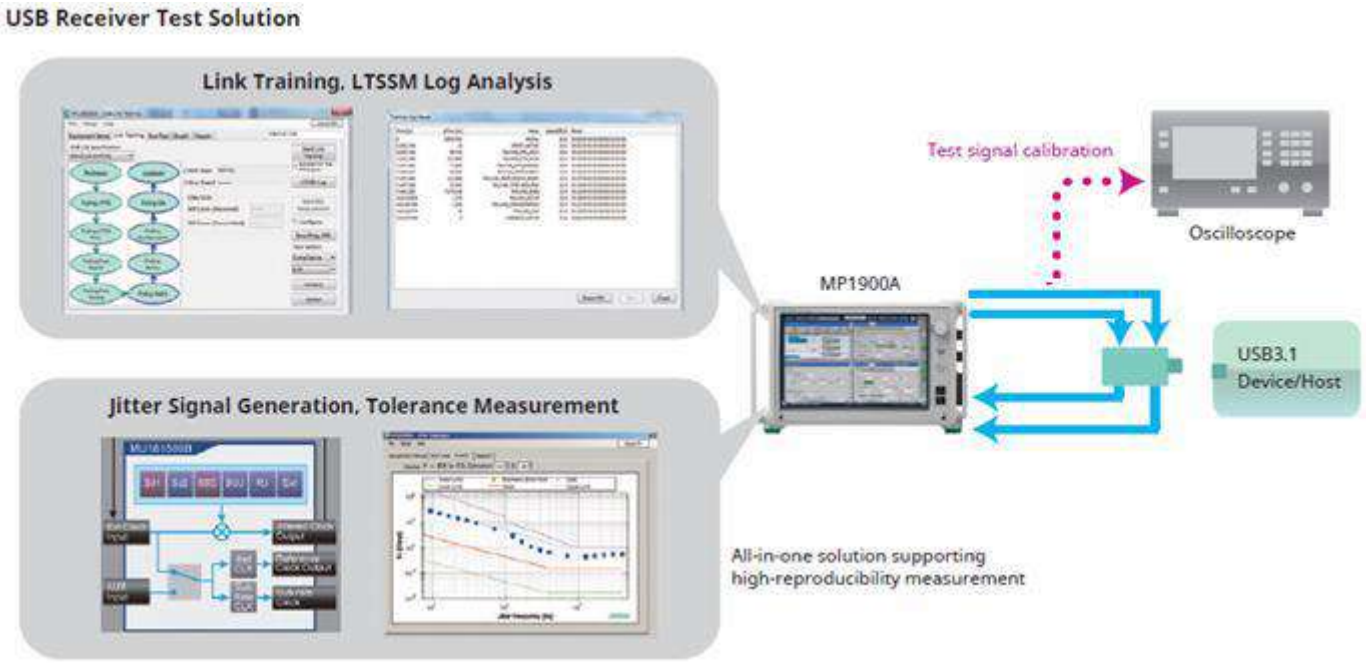
  Supports higher-reproducibility receiver tests

**USB Type-C Receiver Test (USB4, Thunderbolt3)**



# MP1900A Series USB3.2 Receiver Test Solution

- Protocol Aware and All-in-one USB3.2 Rx test solution. Supports USB 3.2 x2.
- Wideband BERT 2.4 Gbit/s to 32.1 Gbit/s supporting PCIe Gen4/5 and Thunderbolt3
- High-quality waveforms with low Intrinsic Jitter, high-reproducibility measurement using high-sensitivity ED
- Link Training and LTSSM analysis function
- Transmit and receive LFPS and LBPM signals
- Insert and identify SKP Ordered Set
- Jitter Addition (SJ, RJ, BUJ, SSC) and Tolerance measurement



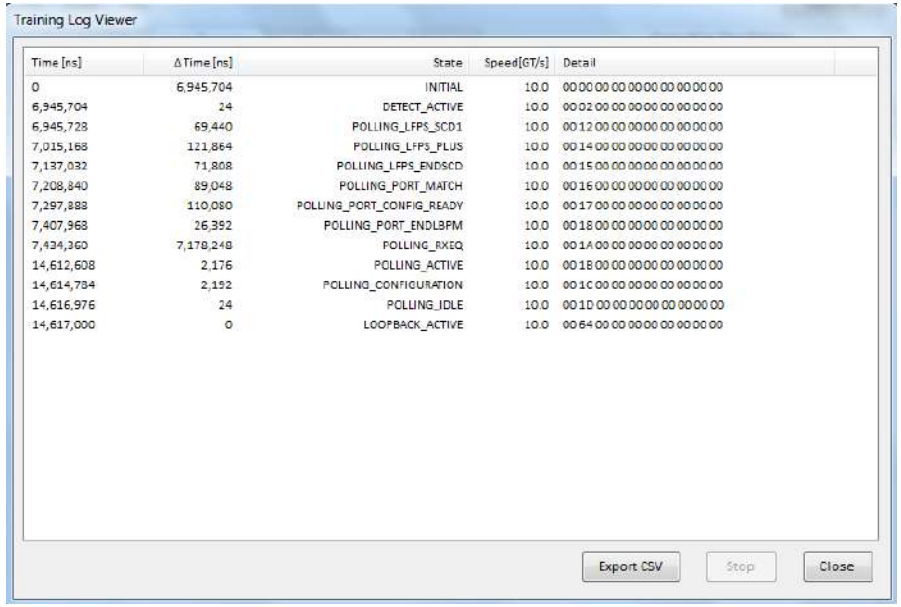
# USB3.2 Link Training, LTSSM Analysis and Jitter Tolerance

Anritsu Advancing beyond

## Shorter Development Period by LTSSM Analysis Function for Troubleshooting Cause of Link Faults

Controls state transition from “Detect” to “Loopback” required by Rx test


For confirming results of each state transition with Training Log Viewer



# USB Type-C Receiver Test Recommended Equipment List (1/2)

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MP1900A | Signal Quality Analyzer-R | - | 1 | |
| MU181000B | 12.5GHz 4port Synthesizer | - | 1 | |
| MU181500B | Jitter Modulation Source | - | 1 | |
| MU195020A | 21G/32G bit/s SI PPG | 010, 011 | 1 | |
| MU195040A* | 21G/32G bit/s SI ED | 010, 011, 022 | 1 | |
| MU195050A | Noise Generator | - | 1 | |
| MX183000A-PL001* | Jitter Tolerance Test | - | 1 | |
| MX183000A-PL022* | USB Link Training | - | 1 | |
| MX183000A-PL023* | USB 3.2 x 2 Link Training | | 1 | Supports USB 3.2 x2<br>Also requires MX183000A-PL022 |
| J1551A | Coaxial Skew Matched Cable (0.8 m) | - | 3 | |
| K261 | DC Block | - | 2 | |
| - | K-SMP Adapter | - | 4 | Recommend part equivalent to Rosenberger 02K119-K00E3 |
| - | ISI Channel | - | 1 | Recommend part equivalent to Tektronix BSA12500 |
| - | USB4/TBT3 Test Fixture | - | 1 | Purchase from Wilder Technology |
| USB31CET* | USB3.1 Type-C Test Fixture | - | 1 | Purchase from USB-IF website |

*These items are required only for USB3.2 test. USB4 and TBT3 don’t need them.

# USB Type-C Receiver Test Recommended Equipment List (2/2)

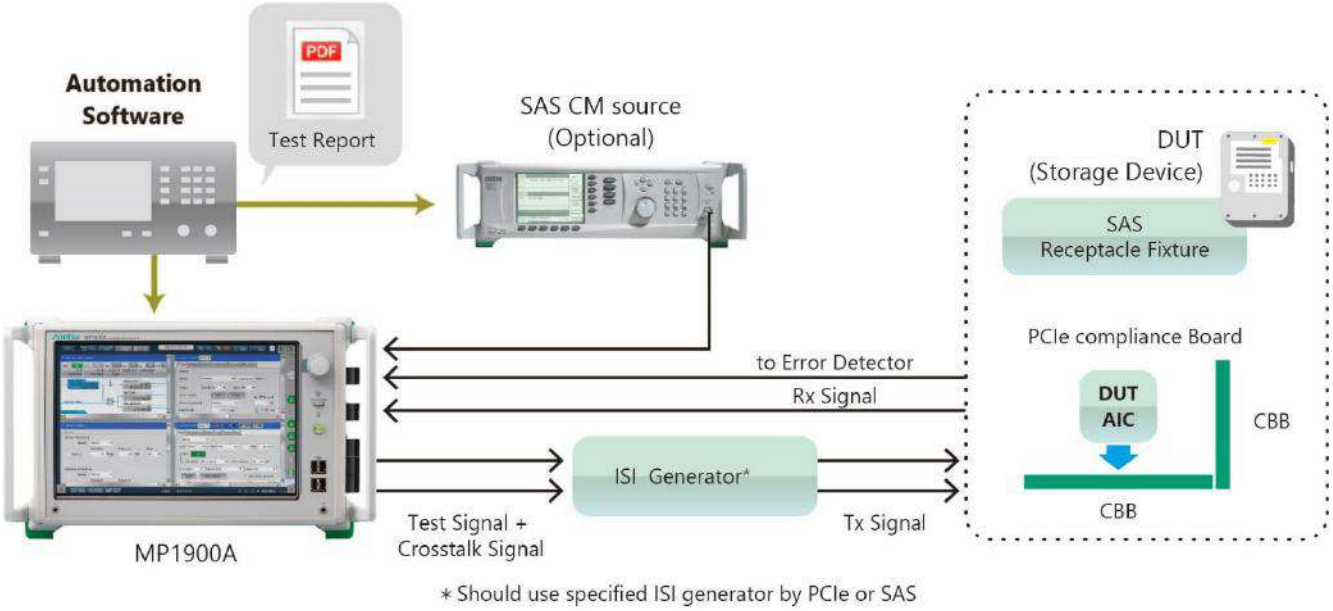
Choose the automation software matching your oscilloscope.

| Model | Electrical Test | Remark |
|---|---|---|
| QPHY-USB4-TX-RX | USB4/TBT3 Tx, Rx | Teledyne LeCroy scope<br>Purchase from Teledyne LeCroy |
| QPHY-USB3.1-Tx-Rx | USB 3.2 Tx, Rx | |
| GRL-USB4-RXA | USB4 Rx | Keysight scope<br>Purchase from Granite River Labs |
| GRL-TBT3-RXA | TBT3 Rx | |
| GRL-USB31-RXA | USB 3.2 Rx | |
| GRL-USB32-RXA | USB 3.2 x2 Rx | |

# SAS Test Solution

# SAS Receiver Test Solution

- Same configuration supports receiver tests of SAS and PCIe.
  Wideband operation from 2.4 Gbit/s to 21 Gbit/s with expansion to 32.1 Gbit/s
  Supports SAS-4 (22.5 Gbit/s) and Gen5 (32G) measurements without changing configuration
- Combination with automation software supports oscilloscope from main makers
  Simplifies complex test procedures and reduces work burden by using own oscilloscope.
- High-performance multichannel BERT with high-quality output waveforms (12-ps Tr/Tf, 115-fs rms Intrinsic Jitter) and high-input sensitivity (15 mV EH)
  Supports higher-reproducibility receiver tests



# SAS Receiver Test Recommended Equipment List (1/2)

Anritsu
Advancing beyond

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MP1900A | Signal Quality Analyzer-R | - | 1 | |
| MU181000B | 12.5GHz 4port Synthesizer | | 1 | |
| MU181500B | Jitter Modulation Source | - | 1 | |
| MU195020A | 21G/32G bit/s SI PPG | 001*, 010, 011, 040 | 1 | *Add Opt-001 for expansion to SAS-4 |
| MU195050A | Noise Generator | - | 1 | |
| MU195040A | 21G/32G bit/s SI ED | 001*, 010, 011, 022 | 1 | *Add Opt-001 for expansion to SAS-4 |
| J1758A | Variable ISI Channel | - | 1 | |
| - | Mated Adapter Fixture Pair | - | 1 | |
| K261 | DC block | - | 2 | |
| MG3692C | 2GHz to 20GHz Signal Generator | - | 1 | for CM tests |
| K241C | RF Splitter | - | 1 | |

Requires cables to connect with other equipment

# SAS Receiver Test Recommended Equipment List (2/2)

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Advancing beyond

Choose the automation software matching your oscilloscope.

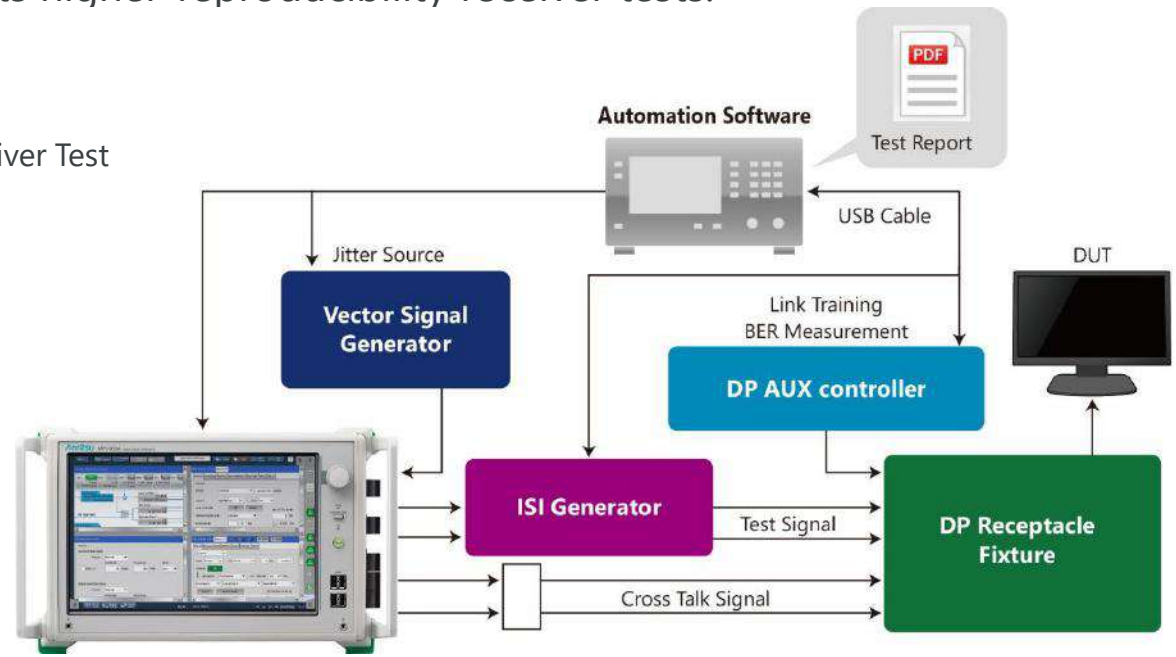
| Model | Measurement item | Remark |
|---|---|---|
| GRL-SAS3-RXA | SAS3 Receiver Calibration and Test | Tektronix or Keysight scope<br>Purchase from Granite River Labs |
| GRL-SAS4-RXA | SAS4 Receiver Calibration and Test | |
| GRL-SAS34-RXA | SAS4 and SAS3 Receiver Calibration and Test | |

# DisplayPort Test Solution

# DisplayPort Receiver Test Solution

- Wideband operation from 2.4 Gbit/s[*1] to 21 Gbit/s with expansion to 32.1 Gbit/s without hardware upgrade
  Flexible support for DisplayPort2.0 (20 Gbit/s) and future faster speeds
  (*1: Can only generate special RBR (1.62 Gbit/s) pattern)
- All-in one Dual-Channel PPG
  True crosstalk effects can be analyzed by controlling inter-channel skew.
- Combination with automation software supports oscilloscope from main makers
  Simplifies complex test procedures and reduces work burden by using own oscilloscope
- High-quality output waveforms (12-ps Tr/Tf, 115-fs rms Intrinsic Jitter) PPG
  Supports higher-reproducibility receiver tests.

DP1.4 SINK Receiver Test



# DisplayPort Receiver Test Recommended Equipment List (1/2)

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MP1900A | Signal Quality Analyzer-R | - | 1 | |
| MU181000B | 12.5GHz 4port Synthesizer | - | 1 | |
| MU181500B | Jitter Modulation Source | - | 1 | |
| MU195020A | 21G/32G bit/s SI PPG | 020, 021 | 1 | |
| MU195050A | Noise Generator | - | 1 | |
| - | Vector Signal Generator | - | 1 | Recommend Regol DSG815 |
| - | ISI Generator | - | 1 | Recommend Artek CLE1000-A2 |
| - | DisplayPort AUX Controller | - | 1 | Recommend Unigraf DPT-200 |
| - | VESA-Approved DisplayPort Mated Adapter Fixture Pair | - | 1 | Recommend Wilder Technology DP-TPA-P DP-TPA-R |
| - | DC Block | - | 2 | Recommend Weinchel Aeroflex Model 7006-1 20GHz |
| - | ÷4 RF Splitter | - | 2 | Recommend Anritsu AN44182A |
| - | TTC (Transition Time Converter) | - | 2 | Recommend HYPERLABS Model # HL9450-60 |
| | | - | 2 | Recommend HYPERLABS Model # HL9450-150 |

Requires cables to connect with other equipment

# DisplayPort Receiver Test Recommended Equipment List (1/2)

| Model | Measurement item | Remark |
|---|---|---|
| GRL-DP14-SINKAN | DisplayPort1.4 SINK | Tektronix or Keysight scope<br>Purchase from Granite River Labs |

# MP1900A PAM4 Applications

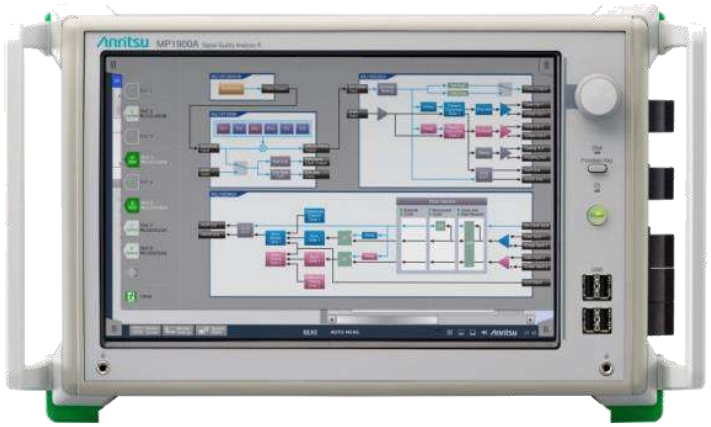
# Outline of MP1900A Series PAM4 BERT

Anritsu
Advancing beyond

- Supports bit error rate measurements optimized for high-speed 400 GbE and next-generation 800 GbE interfaces
- High-quality data output waveforms up to 64 Gbaud and high input sensitivity performance provide strong support for testing PAM4 device designs
- All-in-one Jitter Addition, Clock Recovery, Emphasis, NRZ/PAM3/PAM4 Pattern Editing, SER functions, etc.
- Easily configured, high-reproducibility PAM4 measurement solution

## MP1900A PAM4 Target Applications

200/400/800 GbE, CEI-56G/112G, InfiniBand HDR, 64G Fibre Channel



# MP1900A PAM4 BERT Features

- All-in-one, high-reproducibility, easily configured test solution
- High-quality waveforms for more accurate measurement
- Easy, low-cost, future-proof expandability supporting high bit rates and multichannels

## PAM4 One Box Test Solution

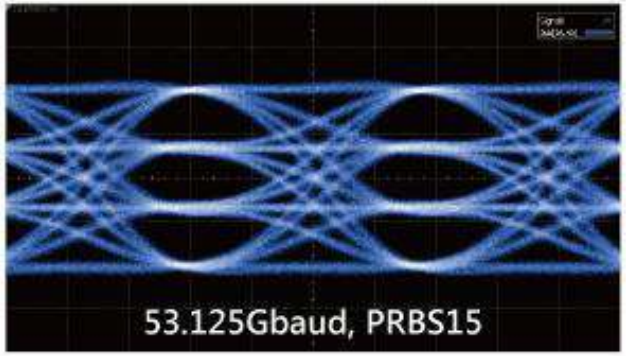
Emphasis 4Tap, 20dB

Built-in Clock Recovery

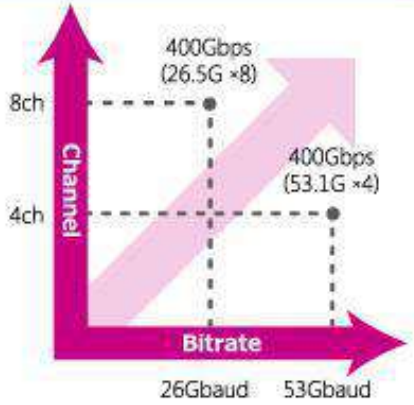
Jitter/Noise Addition

Jitter Tolerance Test

## Highest Level Waveform Quality




## Next-Generation Terabit



# PAM4 All-in-One BERT Solution

Anritsu
Advancing beyond

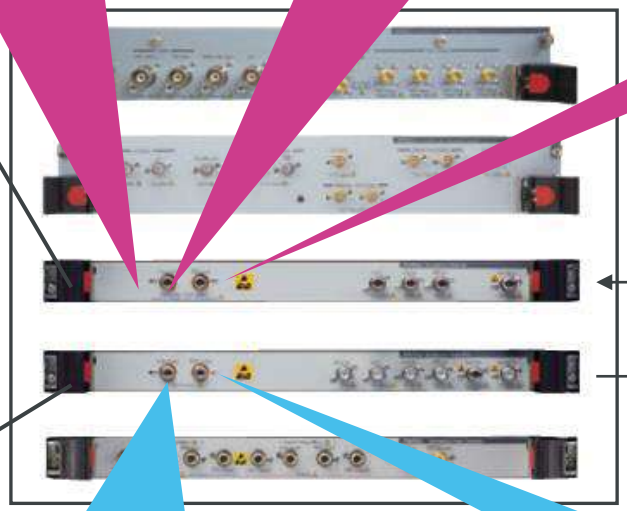
Easy-to-use and configure all-in-one solution with high reproducibility, helping cut test times

Typ. 36 mV at 53.125 G
High Input Sensitivity

ED w/ Built-in Clock
Recovery and Equalizer

SER/BER, Capture,
Logging functions

PAM4 ED
MU196040B



DUT

PAM4 PPG
MU196020A

No External Equipment, Compact Module with Built-in PAM4 Functions

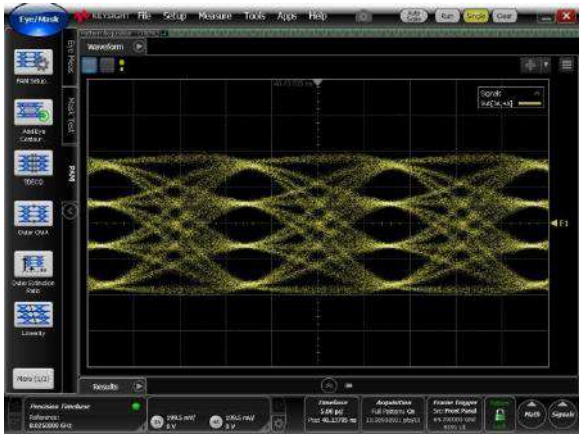
High-Quality 64G PAM4 Waveforms with Variable Emphasis/Linearity Functions

# High-Quality Waveform PAM4 PPG MU196020A

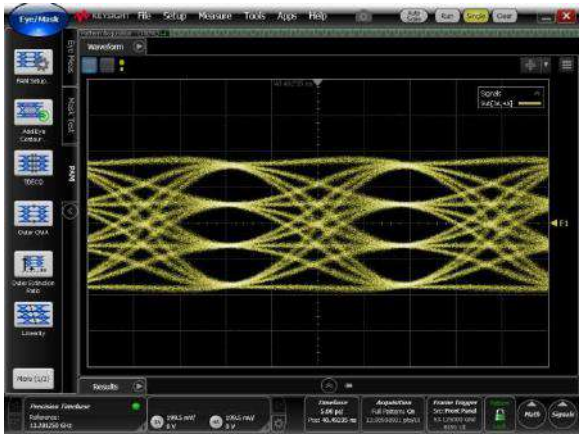
Anritsu
Advancing beyond

Best-in-class waveform quality with low Intrinsic Jitter (typ. 170 fs (rms) and fast Tr/Tf (typ. 8.5 ps) for more accurate evaluation of actual DUT performance

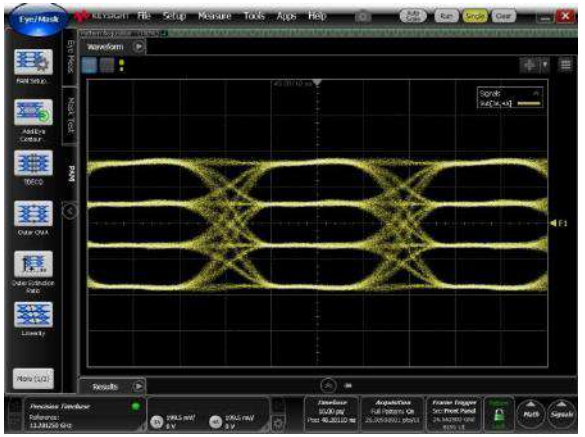
64.2 Gbaud

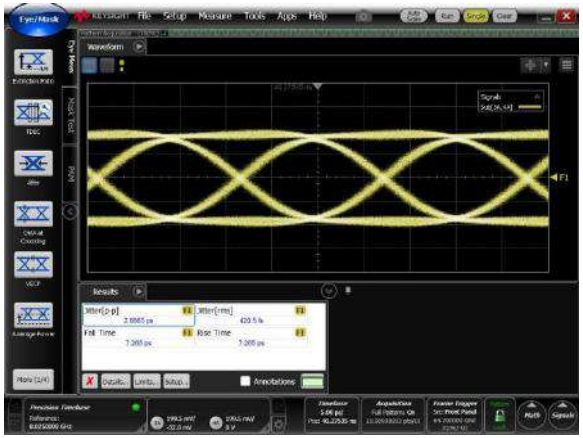


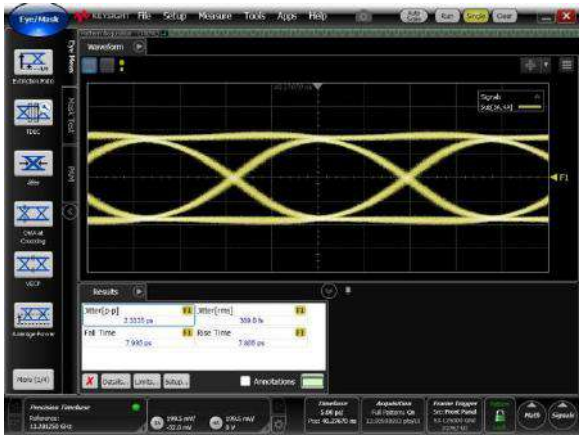
53.125 Gbaud

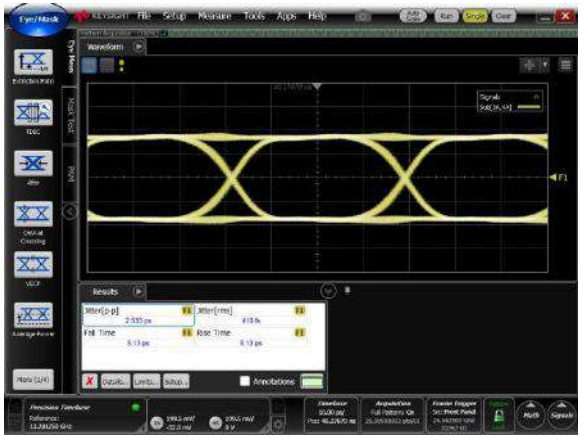


26.5625 Gbaud









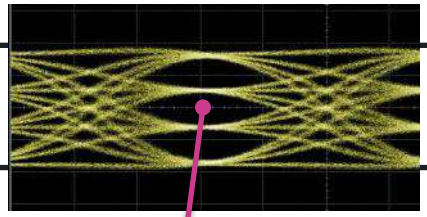
Differential 1.4 Vp-p, PRBS13Q pattern, J1789A 40-cm cable + 70 GHz Scope

# 116 Gbit/s PAM4 Best Level High-Sensitivity Input Performance

High sensitivity input of 36 mV (typical at 53.125 Gbaud) simplifies previously difficult PAM4 error troubleshooting measurements.

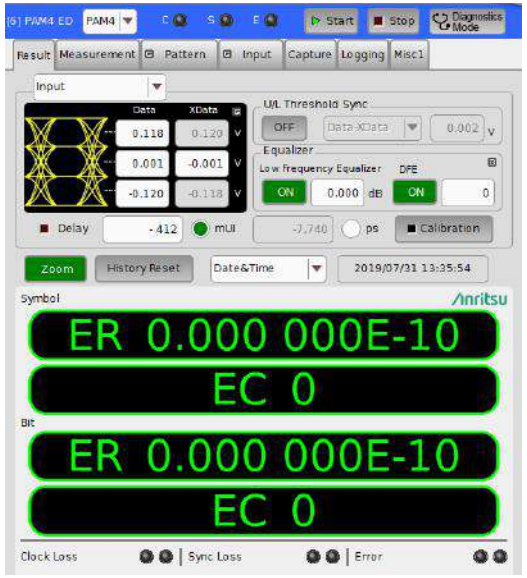
**Error-Free** at 53.125 Gbaud
Best level PAM4 sensitivity

PAM4 PPG
MU196020A



Typ. 36 mV EH/ Eye

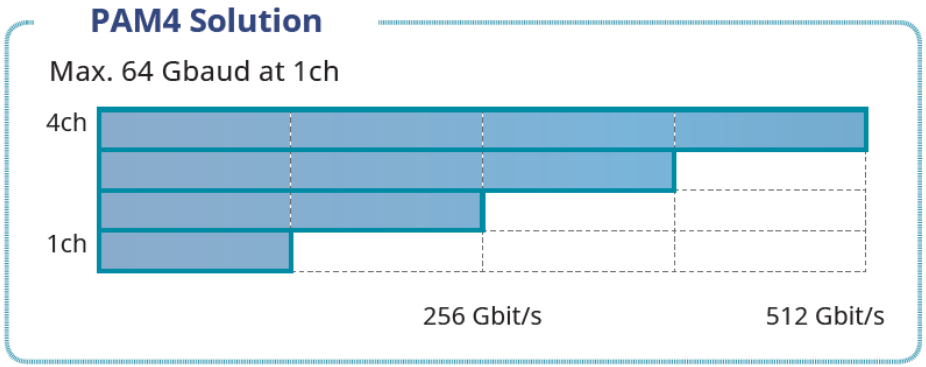
**PAM4 ED**
**MU196040B**



# Multichannel Support and Expandability (1/2)

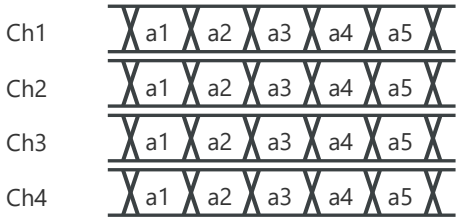
Anritsu
Advancing beyond

One MP1900A PPG supports up to 4ch for 400 GbE (53 Gbaud x 4 Lanes), and faster evaluations, helping cut future support upgrade costs.



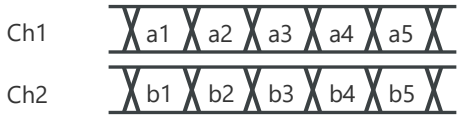

- **Channel Synchronization**

One MP1900A unit supports synchronous output for up to 4ch; two units support up to 8ch.
*Future support for 8ch

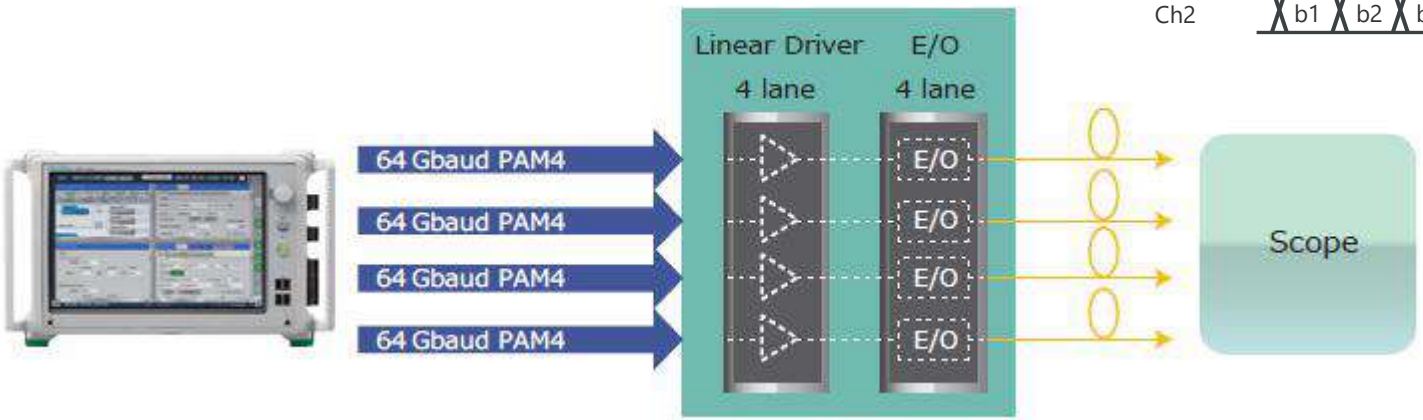



- **2ch Combination (NRZ)**

Supports shift to "a1b1 a2b2 . . ." pattern



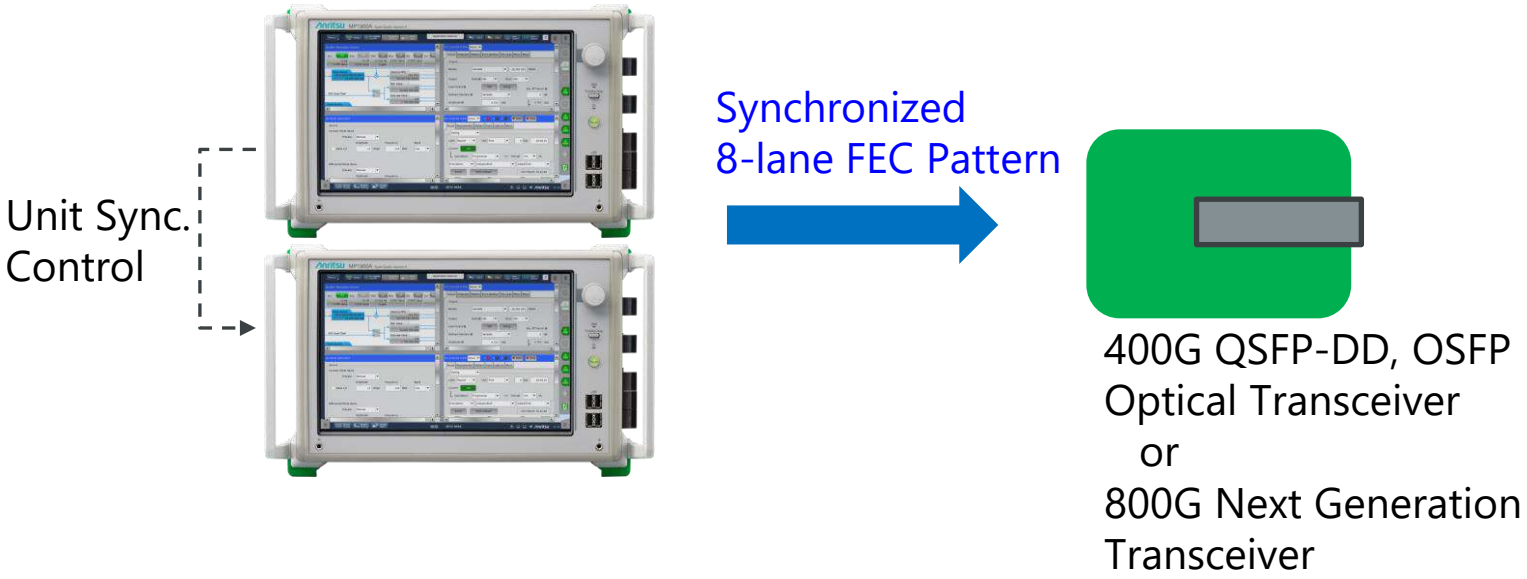

- 4-Lane DUT (Driver + E/O) Measurement Example



# Multichannel Support and Expandability (2/2)

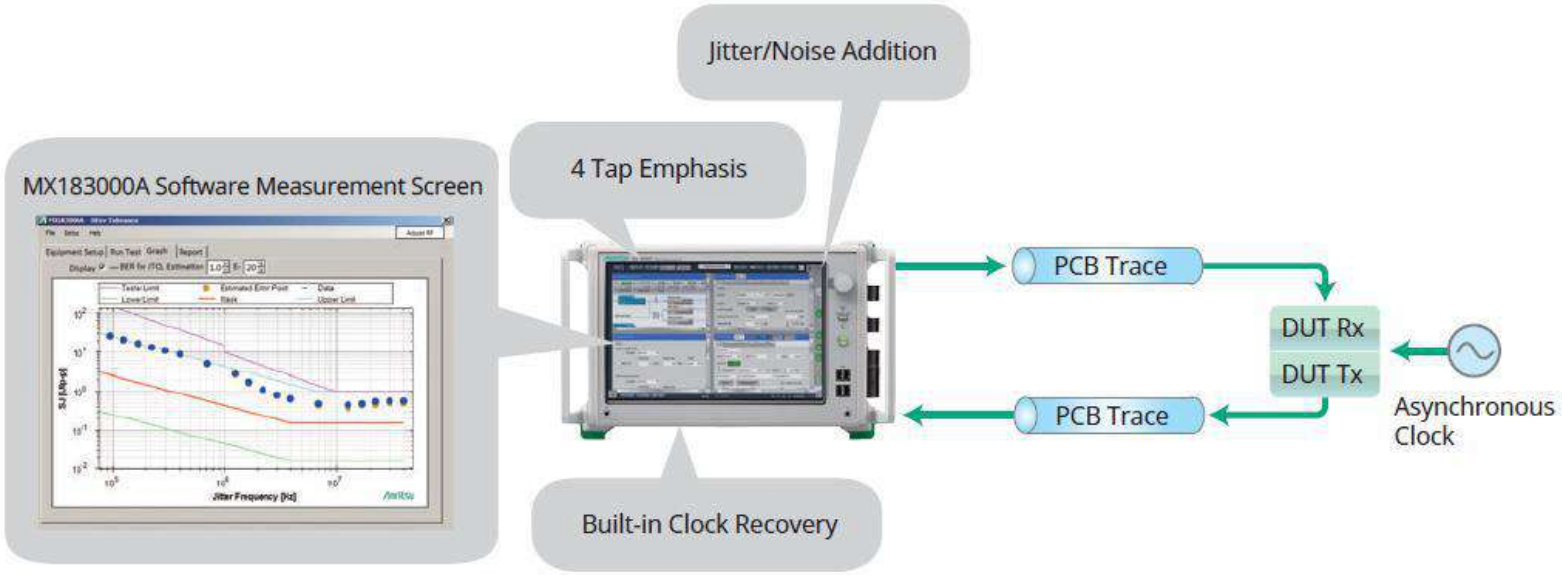
Anritsu
Advancing beyond

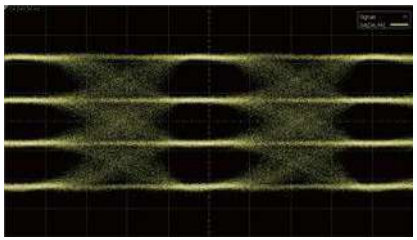
Expanded support for 800G using 8ch synchronization function
(4ch x 53.125 Gbaud PAM4 x two MP1900A units)
Supports QSFP-DD transceiver FEC evaluation using 8-lane FEC Pattern Generation function



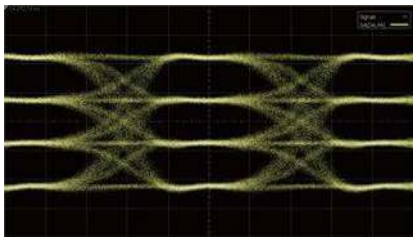
# Jitter Tolerance Measurement Function

Supports PAM4 Jitter Tolerance test using just one unit. A measurement system to help cut measurement time is configured easily by combining the Jitter/Noise Addition function, built-in Clock Recovery function, and Jitter Tolerance MX183000A-PL001 software.

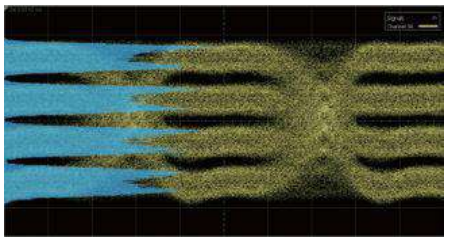


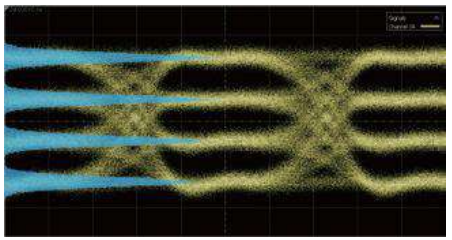
Sine-Wave Jitter (SJ)



Random Jitter (RJ)



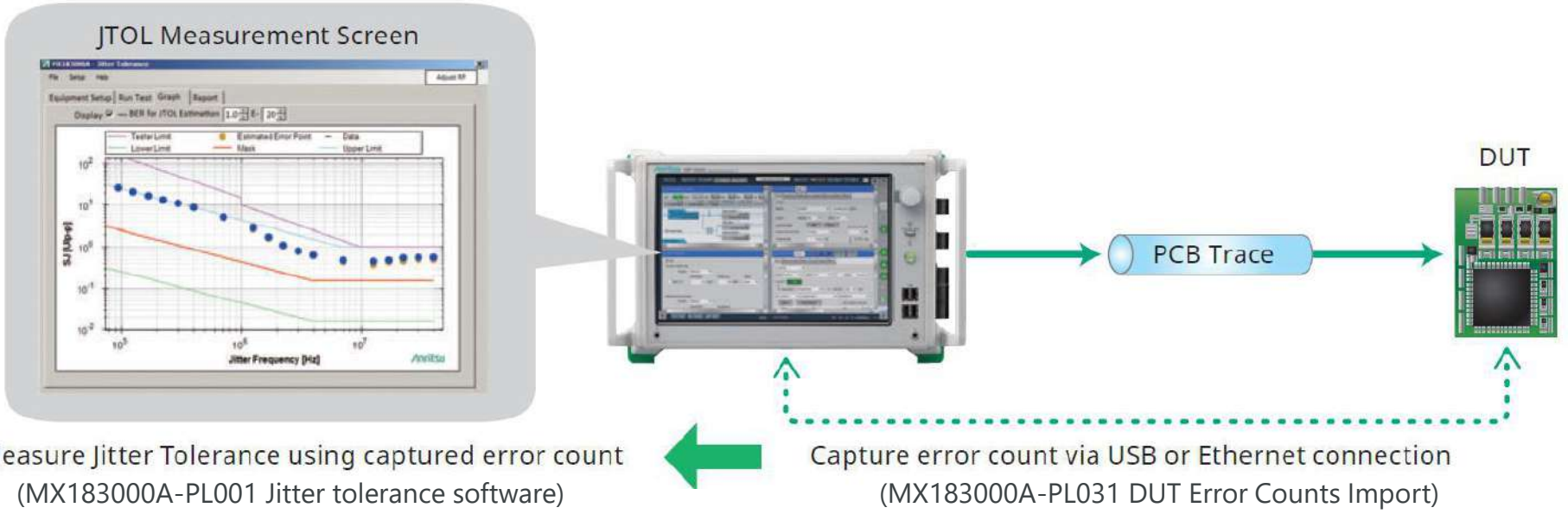
CM/DM Noise



White Noise

# Jitter Tolerance Measurement using DUT BER Counter

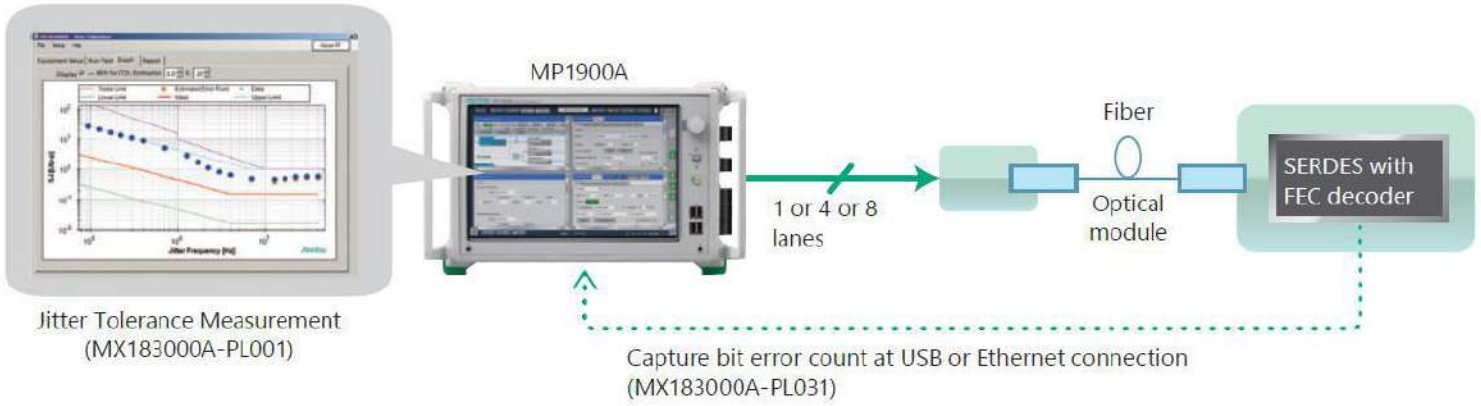
When the DUT has a built-in bit error counter, combination with the MP1900A PPG makes it easy to configure a highly cost-effective Jitter Tolerance measurement environment.



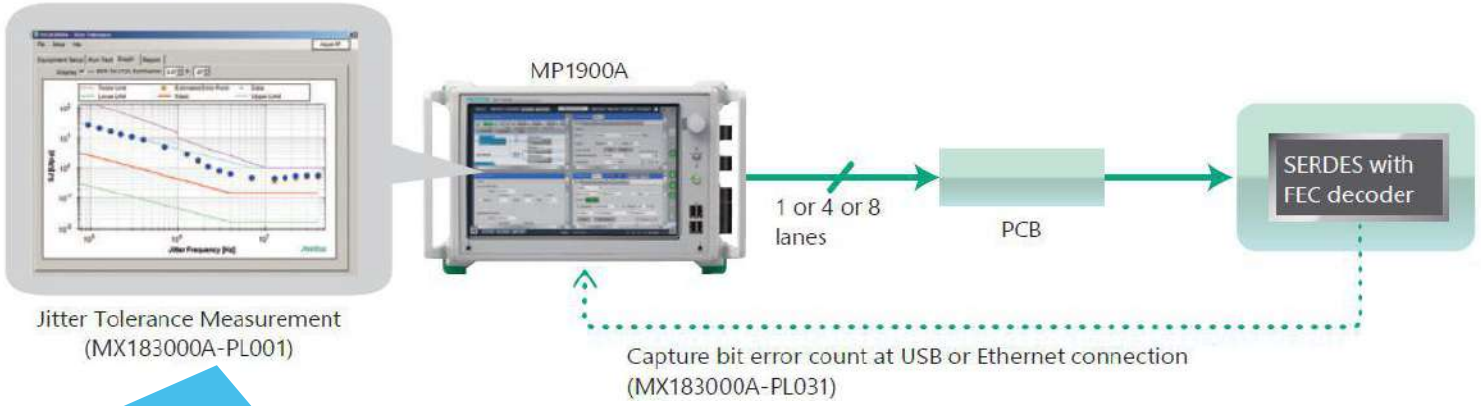
# Multilane FEC Evaluation

FEC can be evaluated by combining FEC pattern generation with error insertion, and reading the DUT bit error count.

**Evaluating Optical FEC Signal Transmission**




**Evaluating Electrical FEC Signal Transmission**




Evaluate Jitter Tolerance, etc., using captured error count

# PAM4 PPG/ED Specifications

## PAM4 PPG MU196020A

- Baud-rate: 2.4 Gbaud to 32.1/58.2/64.2 Gbaud
- Output amplitude: 0.14 Vp-p to 1.6 Vp-p (Differential)
- Emphasis: 4Tap, ±20 dB (1 post/2 pre-cursor), ISI/Channel Emulator
- Intrinsic jitter(rms): 170 fs (typ., NRZ)
- Tr/Tf (20-80%): 8.5 ps (typ., NRZ)
- Multichannel synchronization
- FEC pattern generation

## PAM4 ED MU196040B

- Baud-rate: 2.4 Gbaud to 32.1/58.2 Gbaud PAM4 and 64.2 Gbaud NRZ
- Input amplitude (max.): 1.0 Vp-p (NRZ, PAM4)
- Input sensitivity(Eye Height) : 23 mV (typ., 26.5625 Gbaud), 36 mV (typ., 53.125 Gbaud)
- Built-in Clock Recovery: 2.4 G to 29 Gbaud or 32.1 Gbaud/ 51 G to 58.2 Gbaud extension
- Analog bandwidth: >40 GHz (nominal)
- Built-in Equalizer: Low Frequency Equalizer(2 dB)+DFE(1.4 dB)
- SER measurement, logic error analysis using Diagnostics Mode, Capture , Logging function

# Typical Configuration of 58 Gbaud PPG/ED

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Advancing beyond

| Model | Name | Option | Qty | Remark |
|---|---|---|---|---|
| MP1900A | Signal Quality Analyzer-R | - | 1 | |
| MU181000B | 12.5GHz 4 port Synthesizer | - | 1 | |
| MU181500B | Jitter Modulation Source | - | 1 | For jitter injection |
| MU196020A | PAM4 PPG | 002, 011, 040, 042 | 1 | |
| MU196040B | PAM4 ED | 002, 011, 021, 023, 041 | 1 | |

## Software for jitter tolerance test

| Model | Name |
|---|---|
| MX183000A-PL001 | Jitter Tolerance Test |
| MX183000A-PL031 | DUT Error Counts Import |

## Optional parts

| Model | Name |
|---|---|
| J1789A | Electrical Length Specified cable (0.4m, V connector) |
| J1790A | Electrical Length Specified cable (0.8m, V connector) |
| J1800A | ISI Board V |
| J1793A | Pick OFF Tee (V) |

# Appendix

# Ordering Information

| Model | Name |
|---|---|
| MP1900A | Signal Quality Analyzer-R |
| MU181000B | 12.5GHz 4port Synthesizer |
| MU181000B-002 | SSC Extension |
| MU181500B | Jitter Generation Source |
| MU195020A | 21G/32G bit/s PPG |
| MU195020A-001 | 32Gbit/s Extension |
| MU195020A-010 | 1ch Data Output |
| MU195020A-020 | 2ch Data Output |
| MU195020A-011 | 1ch 10Tap Emphasis |
| MU195020A-021 | 2ch 10Tap Emphasis |
| MU195020A-030 | 1ch Data Delay |
| MU195020A-031 | 2ch Data Delay |
| MU195020A-040 | 1ch Variable ISI |
| MU195020A-041 | 2ch Variable ISI |
| MU195020A-050*1 | Sequence Editor Function |
| MU195020A-051*1 | Sequence Editor Function PCIe 5 Extension |
| MU195040A | 21G/32G bit/s SI ED |
| MU195040A-001 | 32Gbit/s Extension |
| MU195040A-010 | 1ch ED |
| MU195040A-020 | 2ch ED |
| MU195040A-011 | 1ch CTLE |
| MU195040A-021 | 2ch CTLE |
| MU195040A-022 | Clock Recovery |

| Model | Name |
|---|---|
| MU195050A | Noise Generator |
| MU195050A-001 | White Noise |
| MU183020A | 28G/32G bit/s PPG |
| MU183040B | 28G/32G bit/s High Sensitivity ED |
| MX183000A-PL001 | Jitter Tolerance Test |
| MX183000A-PL011 | PCIe Link Sequence |
| MX183000A-PL021 | PCIe Link Training*2 |
| MX183000A-PL025 | PCIe 5 Link Training*2 |
| MX183000A-PL022 | USB Link Training*3 |
| MX183000A-PL023 | USB 3.2 x 2 Link Training*3 |
| MX183000A-PL031 | DUT Error Counts Import |

1: Opt-050 supports PCIe Gen1 to Gen 4, and USB 3.2 x1. Opt-051 supports PCIe Gen5. Opt-050 is required when adding Opt-051.
*2: The PL021 option supports PCIe Gen1 to Gen4. The PL025 option supports PCIe Gen5. PL021 is required to add PL025.
*3: PL022 supports USB 3.2 x1. PL023 supports USB 3.2 x2. PL022 is required to add PL023.

# Main Specifications

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## • Signal Quality Analyzer-R MP1900A

| Item | Specification |
|---|---|
| LCD | 12.1" WXGA 1280 x 800 |
| Remote interface | GPIB, LAN |
| Module slots | 8 |
| External equipment interface | USB x6, VGA x1, HDMI x1 |
| OS | Windows 10 IoT Enterprise |
| Power supply | 100 V(ac) to 120 V(ac)/200 V(ac)to 240 V(ac)<br>50 Hz to 60 Hz |
| Power consumption | 1350 VA max. |
| Size and mass | 340 (W) x 222.5 (H) x 451 (D) mm<br>20 kg max. (excluding modules) |

## • 21G/32G bit/s SI ED MU195040A

| Item | Specification |
|---|---|
| Operation bit rate | 2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s |
| Number of channels | 1 or 2 |
| Input attitude | 0.05 Vp-p to 1.0 Vp-p (Single-End)<br>0.1 Vp-p to 2.0 Vp-p (Differential) |
| Input sensitivity | 15 mV (Eye Height 28.1 Gbit/s) |
| CTLE | Peak Frequency 14, 8, 4 GHz<br>Gain 0 to –12 dB |
| Clock Recovery | Yes, supports SSC input |
| PCIe/USB Link Training | Supported (MX183000A-PL021(PCIe),<br>MX183000A-PL022(USB)) |
| I/O connectors | K (f) |

## • 21G/32G bit/s SI PPG MU195020A

| Item | Specification |
|---|---|
| Operation bit rate | 2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s |
| Number of channels | 1 or 2 |
| Output amplitude | 0.1 Vp-p to 1.3 Vp-p (Single-end)<br>0.2 Vp-p to 2.6 Vp-p (Differential) |
| Emphasis | 10Tap |
| Variable ISI | ISI and Channel Emulation functions |
| Tr/Tf (20% to 80%) | 12 ps (typ.) |
| Random tutor | 115 fs rms (typ.) |
| PCIe/USB Link Training | Supported (MX183000A-PL021(PCIe),<br>PL025(PCIe 5), PL022(USB)) |
| I/O connectors | K (f) |

## • Noise Generator MU195050A

| Item | Specification |
|---|---|
| Number of channels | 2 |
| Insertion loss | –3 dB |
| CMI | 0.1 GHz to 1 GHz/1 GHz to 6 GHz |
| DMI | 2 GHz to 10 GHz |
| White Noise | 10 MHz to 10 GHz |
| Crest Factor | >5 |

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