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# PXle-6368 Specifications

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# PXIe-6368 Specifications

The following specifications are typical at 25 °C, unless otherwise noted. For more information about the PXIe-6368, refer to the **X Series User Manual** available from [ni.com/manuals](http://ni.com/manuals).

## Analog Input

Number of channels	16 differential
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the <a href="#">AI Absolute Accuracy</a> section.
<b>Sample rate</b>	
Single channel maximum	2.00 MS/s
Minimum	No minimum
Timing resolution	10 ns
Timing accuracy	50 ppm of sample rate
Input coupling	DC
Input range	±1 V, ±2 V, ±5 V, ±10 V
<b>Maximum working voltage for all analog inputs</b>	
Positive input (AI+)	±11 V for all ranges, Measurement Category I

Negative input (AI-)	$\pm 11$ V for all ranges, Measurement Category I
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**Caution** Do not use for measurements within Categories II, III, and IV.

CMRR (at 60 Hz)	75 dB
Bandwidth	1 MHz
THD	-80 dBFS
<b>Input impedance</b>	
<b>Device on</b>	
AI+ to AI GND	>100 G $\Omega$ in parallel with 100 pF
AI- to AI GND	>100 G $\Omega$ in parallel with 100 pF
<b>Device off</b>	
AI+ to AI GND	2 k $\Omega$
AI- to AI GND	2 k $\Omega$
Input bias current	$\pm 10$ pA
<b>Crosstalk (at 100 kHz)</b>	
Adjacent channels	-80 dB
Non-adjacent channels	-100 dB
Input FIFO size	8,182 samples shared among channels used
Data transfers	DMA (scatter-gather), programmed I/O
<b>Overvoltage protection for all analog input channels</b>	

Device on	±36 V
Device off	±15 V
Input current during overvoltage conditions	±20 mA max/AI pin

## Analog Triggers

Number of triggers	1
Source	AI <0..15>, APFI <0, 1>
Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
<b>Source level</b>	
AI <0..15>	±Full scale
APFI <0, 1>	±10 V
Resolution	16 bits
Modes	Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering
<b>Bandwidth (-3 dB)</b>	
AI <0..15>	3.4 MHz
APFI <0, 1>	3.9 MHz
Accuracy	±1% of range
<b>APFI &lt;0, 1&gt; characteristics</b>	

Input impedance	10 k $\Omega$
Coupling	DC
Protection, power on	$\pm 30$ V
Protection, power off	$\pm 15$ V

## AI Absolute Accuracy

**Table 1.** AI Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Offset Tempco (ppm of Range/ $^{\circ}$ C)	Random Noise, $\sigma$ ( $\mu$ Vrms)	Absolute Accuracy at Full Scale ( $\mu$ V)
10	-10	114	35	252	2,688
5	-5	120	36	134	1,379
2	-2	120	42	71	564
1	-1	138	50	61	313



**Note** For more information about absolute accuracy at full scale, refer to the [AI Absolute Accuracy Example](#) section.

Gain tempco	8 ppm/ $^{\circ}$ C
Reference tempco	5 ppm/ $^{\circ}$ C
Residual offset error	15 ppm of range
INL error	46 ppm of range



**Note** Accuracies listed are valid for up to two years from the device external calibration.

## AI Absolute Accuracy Equation

$$\text{AbsoluteAccuracy} = \text{Reading} \cdot (\text{GainError}) + \text{Range} \cdot (\text{OffsetError}) + \text{NoiseUncertainty}$$

- **GainError** = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
- **OffsetError** = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INLError
- **NoiseUncertainty** = 
$$\frac{\text{Random Noise} \cdot 3}{\sqrt{10,000}}$$
 for a coverage factor of 3  $\sigma$  and averaging 10,000 points.

## AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- **TempChangeFromLastExternalCal** = 10 °C
- **TempChangeFromLastInternalCal** = 1 °C
- **number\_of\_readings** = 10,000
- **CoverageFactor** = 3  $\sigma$

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- **GainError** = 114 ppm + 8 ppm · 1 + 5 ppm · 10 = 172 ppm
- **OffsetError** = 15 ppm + 35 ppm · 1 + 46 ppm = 96 ppm
- **Noise Uncertainty** = 
$$\frac{252 \mu V \cdot 3}{\sqrt{10,000}} = 7.6 \mu V$$
- **AbsoluteAccuracy** = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty = 2688  $\mu V$

## Analog Output

Number of channels	4
DAC resolution	16 bits
DNL	$\pm 1$ LSB, max
Monotonicity	16 bit guaranteed
Accuracy	Refer to the <a href="#">AO Absolute Accuracy</a> section.
<b>Maximum update rate (simultaneous)</b>	
1 channel	3.3 MS/s
2 channels	3.3 MS/s
3 channels	3.3 MS/s
4 channels	3.3 MS/s
Minimum update rate	No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	10 ns
Output range	$\pm 10$ V, $\pm 5$ V, $\pm$ external reference on APFI <0, 1>
Output coupling	DC
Output impedance	0.4 $\Omega$



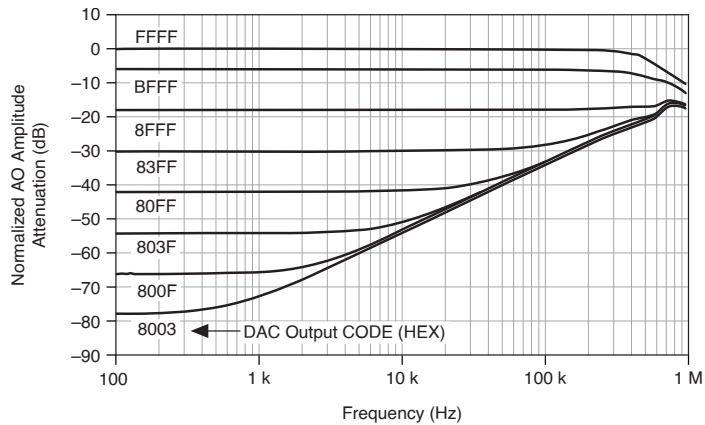
Output current drive	$\pm 5$ mA
Overdrive protection	$\pm 25$ V
Overdrive current	10 mA
Power-on state	$\pm 5$ mV
Power-on/off glitch	1.5 V peak for 200 ms
Output FIFO size	8,191 samples shared among channels used
Data transfers	DMA (scatter-gather), programmed I/O
AO waveform modes	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full-scale step, 15 ppm (1 LSB)	2 $\mu$ s
Slew rate	20 V/ $\mu$ s
Glitch energy at midscale transition, $\pm 10$ V range	6 nV $\cdot$ s

## External Reference

<b>APFI &lt;0, 1&gt; characteristics</b>	
Input impedance	10 k $\Omega$
Coupling	DC
Protection, device on	$\pm 30$ V

Protection, device off	$\pm 15\text{ V}$
Range	$\pm 11\text{ V}$
Slew rate	$20\text{ V}/\mu\text{s}$

**Figure 1.** Analog Output External Reference Bandwidth



## AO Absolute Accuracy

Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within  $10\text{ }^{\circ}\text{C}$  of the last external calibration.

**Table 2.** AO Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/ $^{\circ}\text{C}$ )	Reference Tempco (ppm/ $^{\circ}\text{C}$ )	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/ $^{\circ}\text{C}$ )	INL Error (ppm of Range)	Absolute Accuracy at Full Scale ( $\mu\text{V}$ )
10	-10	129	17	5	65	1	64	3,256
5	-5	135	8	5	65	1	64	1,616



**Note** Accuracies listed are valid for up to two years from the device external calibration.

## AO Absolute Accuracy Equation

$$\text{AbsoluteAccuracy} = \text{OutputValue} \cdot (\text{GainError}) + \text{Range} \cdot (\text{OffsetError})$$

- **GainError** = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
- **OffsetError** = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INLError

## Digital I/O/PFI

### Static Characteristics

Number of channels	48 total, 32 (P0.<0..31>, 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection	±20 V on up to two pins



**Caution** Stresses beyond those listed under the **Input voltage protection** specification may cause permanent damage to the device.

### Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..31>)
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Port/sample size	Up to 32 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	255 samples
DI Sample Clock frequency	0 to 10 MHz, system and bus activity dependent
<b>DO Sample Clock frequency</b>	
Regenerate from FIFO	0 to 10 MHz
Streaming from memory	0 to 10 MHz, system and bus activity dependent
Data transfers	DMA (scatter-gather), programmed I/O
Digital line filter settings	160 ns, 10.24 $\mu$ s, 5.12 ms, disable

## PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	90 ns, 5.12 $\mu$ s, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

## Recommended Operating Conditions

<b>Input high voltage (<math>V_{IH}</math>)</b>	
Minimum	2.2 V

Maximum	5.25 V
<b>Input low voltage (<math>V_{IL}</math>)</b>	
Minimum	0 V
Maximum	0.8 V
<b>Output high current (<math>I_{OH}</math>)</b>	
P0.<0..7>	-24 mA maximum
PFI <0..15>/P1/P2	-16 mA maximum
<b>Output low current (<math>I_{OL}</math>)</b>	
P0.<0..7>	24 mA maximum
PFI <0..15>/P1/P2	16 mA maximum

## Digital I/O Characteristics

Positive-going threshold ( $V_{T+}$ )	2.2 V maximum
Negative-going threshold ( $V_{T-}$ )	0.8 V minimum
Delta VT hysteresis ( $V_{T+} - V_{T-}$ )	0.2 V minimum
$I_{IL}$ input low current ( $V_{IN} = 0$ V)	-10 $\mu$ A maximum
$I_{IH}$ input high current ( $V_{IN} = 5$ V)	250 $\mu$ A maximum

Figure 2. P0.<0..31>:  $I_{OH}$  versus  $V_{OH}$

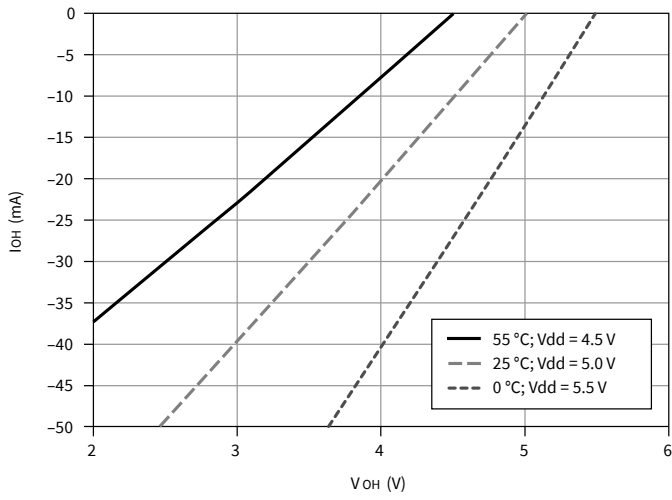


Figure 3. P0.<0..31>:  $I_{OL}$  versus  $V_{OL}$

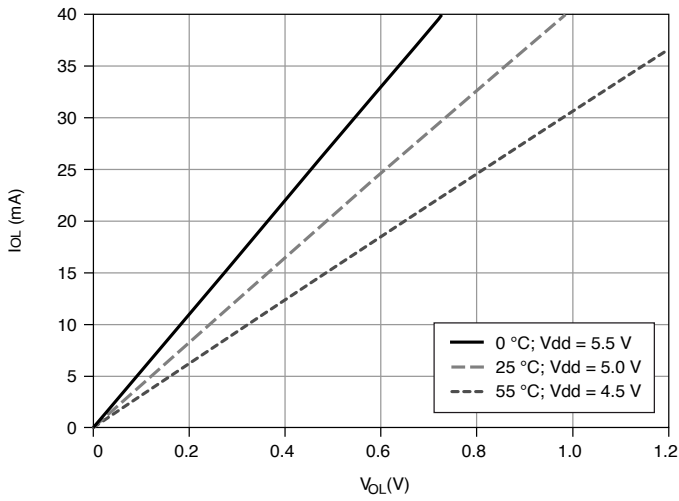
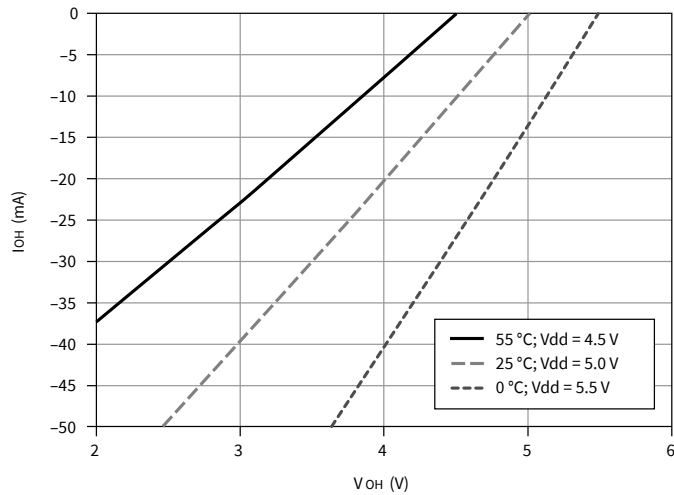
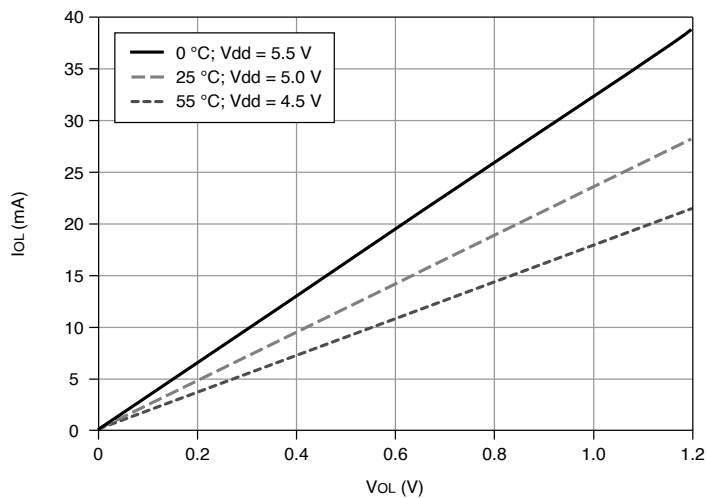


Figure 4. PFI <0..15>/P1/P2:  $I_{OH}$  versus  $V_{OH}$ Figure 5. PFI <0..15>/P1/P2:  $I_{OL}$  versus  $V_{OL}$ 

## General-Purpose Counters

Number of counter/timers	4
Resolution	32 bits
Counter measurements	Edge counting, pulse, pulse width, semi-period, period, two-edge separation

Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	100 MHz, 20 MHz, 100 kHz
External base clock frequency	0 MHz to 25 MHz; 0 MHz to 100 MHz on PXIe_DSTAR<A,B>
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Routing options for inputs	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR, analog trigger, many internal triggers
FIFO	127 samples per counter
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O

## Frequency Generator

Number of channels	1
Base clocks	20 MHz, 10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm



Output can be available on any PFI terminal.

## Phase-Locked Loop (PLL)

Number of PLLs	1
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**Table 3.** Reference Clock Locking Frequencies

Reference Signal	PXI Express Locking Input Frequency (MHz)
PXIe_DSTAR<A,B>	10, 20, 100
PXI_STAR	10, 20
PXIe_CLK100	100
PXI_TRIG <0..7>	10, 20
PFI <0..15>	10, 20
Output of PLL	100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases

## External Digital Triggers

Source	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Digital waveform generation (DO) function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Digital waveform acquisition (DI) function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

## Device-to-Device Trigger Bus

Input source	PXI_TRIG <0..7>, PXI_STAR, PXIe_DSTAR<A,B>
Output destination	PXI_TRIG <0..7>, PXIe_DSTARC
Output selections	10 MHz Clock, frequency generator output; many internal signals
Debounce filter settings	90 ns, 5.12 $\mu$ s, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

## Bus Interface

Form factor	x1 PXI Express peripheral module, specification rev 1.0 compliant
Slot compatibility	x1 and x4 PXI Express or PXI Express hybrid slots
DMA channels	8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

All PXIe devices may be installed in PXI Express slots or PXI Express hybrid slots.

## Power Requirements



**Caution** The protection provided by the device can be impaired if the device is used in a manner not described in the **X Series User Manual**.

+3.3 V	8.2 W
+12 V	21.8 W

## Current Limits



**Caution** Exceeding the current limits may cause unpredictable device behavior.

+5 V terminal (connector 0)	1 A max <sup>[1]</sup>
+5 V terminal (connector 1)	1 A max <sup>[1]</sup>
P0/PFI/P1/P2 and +5 V terminals combined	1.7 A max

## Physical Characteristics

PXIe printed circuit board dimensions	Standard 3U PXI
Weight	241 g (8.5 oz)
I/O connectors	2 68-pin VHDCI

**Table 4.** PXIe Mating Connectors

Manufacturer, Part Number	Description
MOLEX 71430-0011	68-Pos Right Angle Single Stack PCB-Mount VHDCI (Receptacle)
MOLEX 74337-0016	68-Pos Right Angle Dual Stack PCB-Mount VHDCI (Receptacle)
MOLEX 71425-3001	68-Pos Offset IDC Cable Connector (Plug) (SHC68-*)
USB screw terminal/BNC screw terminal wiring	16-24 AWG

## Calibration

Recommended warm-up time	15 minutes
Calibration interval	2 years

## Maximum Working Voltage

**Maximum working voltage** refers to the signal voltage plus the common-mode voltage.

Channel to earth	11 V, Measurement Category I
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**Caution** Do not use for measurements within Categories II, III, or IV.

## Shock and Vibration

Operational shock	30 g peak, half-sine, 11 ms pulse
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	(Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
<b>Random vibration</b>	
Operating	5 to 500 Hz, 0.3 g <sub>rms</sub>
Nonoperating	5 to 500 Hz, 2.4 g <sub>rms</sub>  (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

## Environmental

Operating temperature	0 to 55 °C
Storage temperature	-40 to 70 °C
Operating humidity	10 to 90% RH, noncondensing
Storage humidity	5 to 95% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m

Indoor use only.

## Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1



**Note** For safety certifications, refer to the product label or the [Product Certifications and Declarations](#) section.

## EMC Standards

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- ICES-001: Class A emissions



**Note** Group 1 equipment is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



**Note** In Europe, Australia, New Zealand, and Canada (per CISPR 11) Class A equipment is intended for use in non-residential locations.

## CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

## Product Certifications and Declarations


Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit [ni.com/product-certifications](https://ni.com/product-certifications), search by model number, and click the appropriate link.

## Environmental Management


NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at [ni.com/environment](https://ni.com/environment). This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

## EU and UK Customers

-  **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit [ni.com/environment/weee](https://ni.com/environment/weee).

## 电子信息产品污染控制管理办法（中国 RoHS）

-  **中国 RoHS**—NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 [ni.com/environment/rohs\\_china](https://ni.com/environment/rohs_china)。(For information about China RoHS compliance, go to [ni.com/environment/rohs\\_china](https://ni.com/environment/rohs_china).)

# Device Pinout

Figure 6. NI PXle-6368 Pinout

