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FEC Analysis MU196040B-x42

PAM4 ED MU196040B

Signal Quality Analyzer-R

MP1900A Series

SQA-R

Background

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Data centers supporting next-generation, high-speed, large-capacity 5G mobile communications are progressing with introduction of equipment meeting the 400 GbE communications standard, while also starting investigation of 800 GbE and 1.6 TbE standards to facilitate even faster speeds.

The PAM4 transmission method used by 400 GbE expresses digital data using four voltage levels per unit time to transmit twice as much data compared to the earlier conventional NRZ method. However, due to the narrower differences between the four voltage levels, the greater susceptibility to noise and transmission-path losses makes error-free transmission more difficult than using the conventional NRZ method. As a result, error correction using FEC is applied to assure transmission quality. Consequently, evaluation of devices and transceivers supporting PAM4 not only requires jitter tolerance and sensitivity evaluations based on conventional bit error and error-free measurements, but also requires measurement of error-correction capability using FEC.

Features of FEC Analysis Function

- Detects both bit errors and FEC Symbol Errors in real-time
- Measures jitter tolerance referenced to FEC Symbol Error count as a pass/fail criterion
- Displays distribution of FEC Symbol Errors per Codeword in real-time
- Supports input signal capture at timing exceeding FEC symbol threshold to debug burst errors

[Target Applications] 50, 100, 200, 400, and 800 GbE

High-sensitivity 116-Gbit/s PAM4 ED supports reliable FEC Symbol Error measurements

MP1900A PAM4 BERT

PAM4 Test Signal with Jitter

Test Board

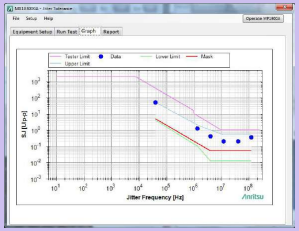
PHY IC

Real-time FEC Symbol Error Measurement

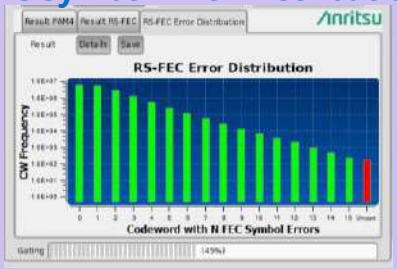
Result PAM4 | Result RS-FEC

		Uncorr. Codeword	FEC Symbol	Bit		
				Total	INS	OMI
MSB	ER		2.192 300E-06	2.199 500E-07	4.382 900E-07	1.555 200E-09
	EC		25 623	26 876	26 781	95
LSB	ER		2.728 900E-03	2.758 500E-04	4.223 500E-04	1.293 100E-04
	EC		3.189 400E+07	3.223 900E+07	2.468 300E+07	7 556 450
MSB + LSB	ER	0.000 000E-00	1.365 500E-03	1.381 200E-04	2.116 100E-04	6.462 300E-05
	EC	0	3.192 000E+07	3.375 500E+07	2.586 000E+07	7 895 263

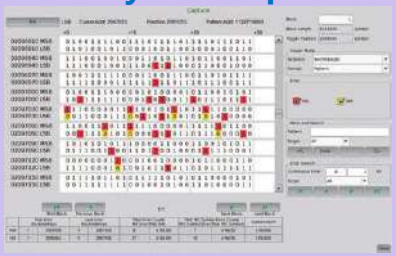
Jitter Tolerance Test Based on Correctable/Uncorrectable FEC



FEC Symbol Error Distribution



FEC Symbol Capture



Real-time FEC Symbol Error Measurement

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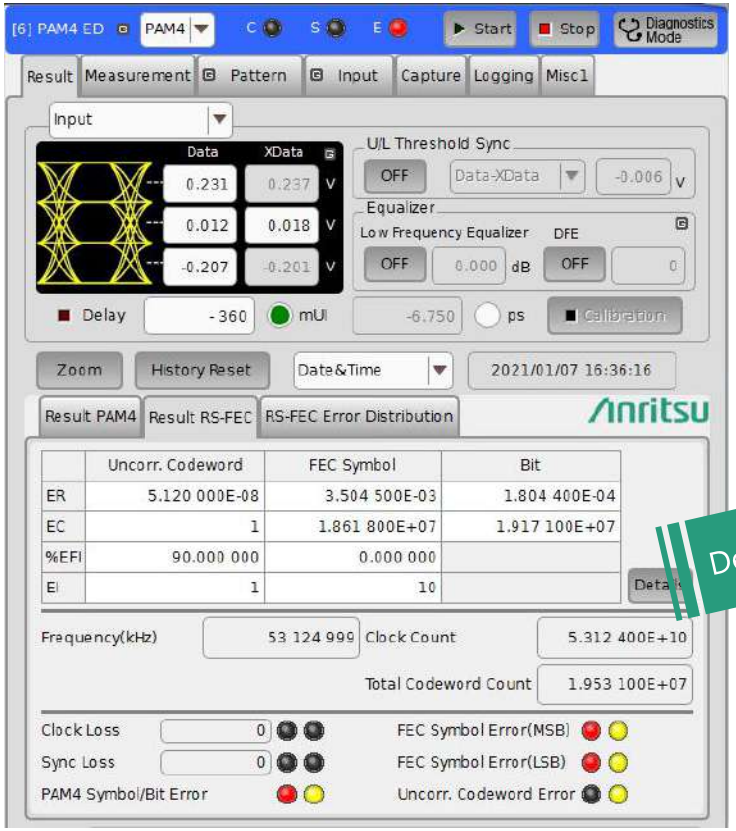
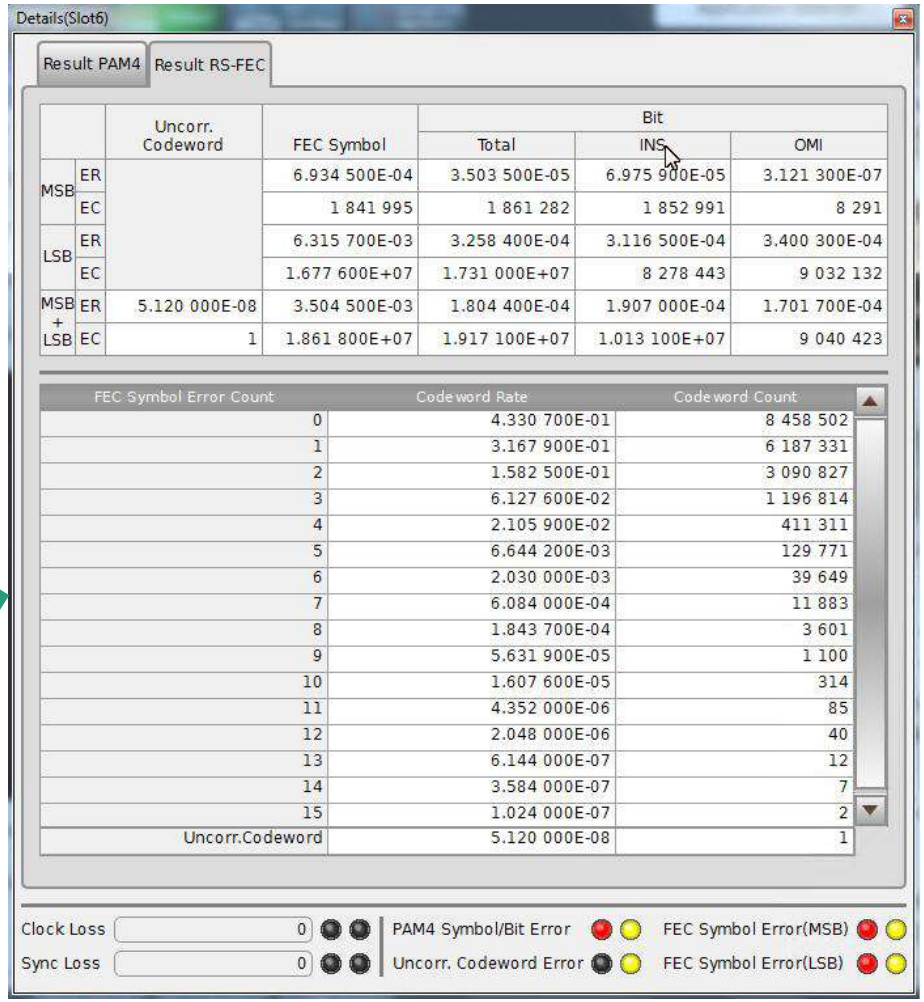
Uncorrectable Codeword, FEC Symbol Error, and Bit Error measurement results on one screen

MU196040B PAM4 ED Result Screen



Details

MSB/LSB Errors and Codeword Counts and Rate for each Symbol Error Count on Details Screen



Jitter Tolerance Measurements Based on FEC Symbol Errors

Sample Video

One-button jitter tolerance measurement is supported based on whether or not error correction using FEC is possible.

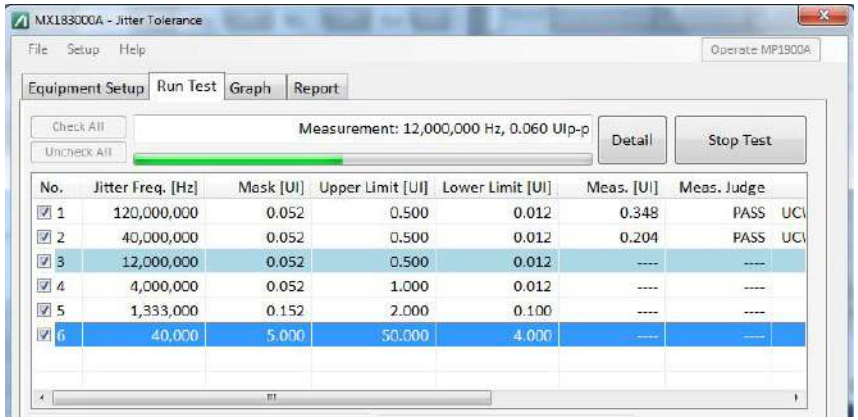
MP1900A PAM4 BERT

PAM4 Test Signal with Jitter

Test Board

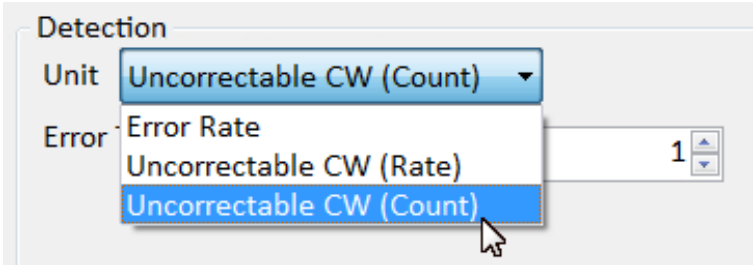
PHY IC

Jitter Frequency and Test Mask Settings

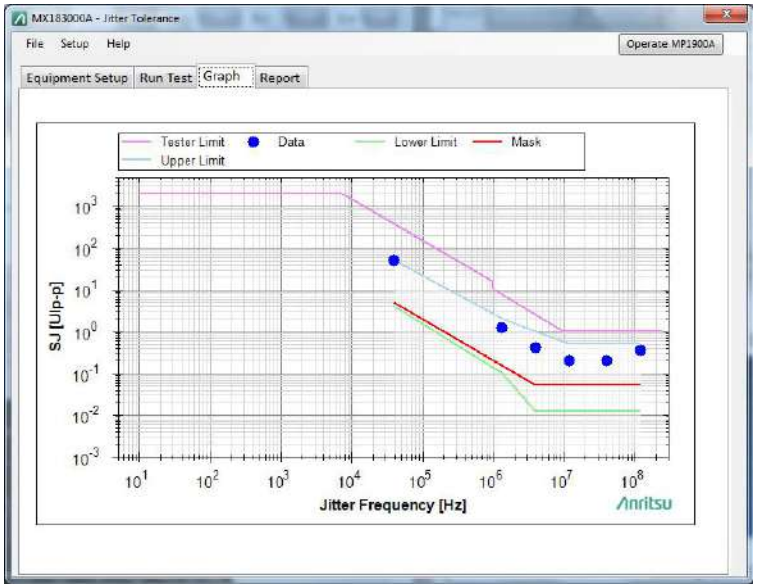


Start Test

Test Criterion Setting, Bit Error or Uncorrectable Codeword



Correctable Error Jitter Tolerance Test Result



FEC Symbol Error Distribution in Real-time

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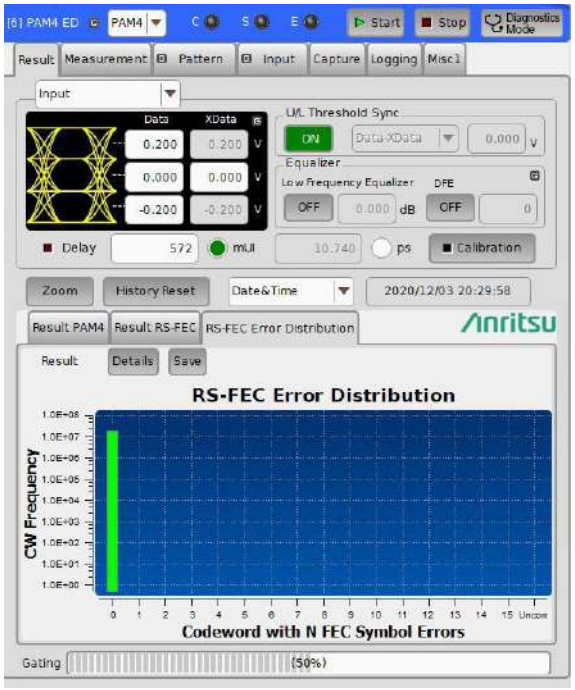
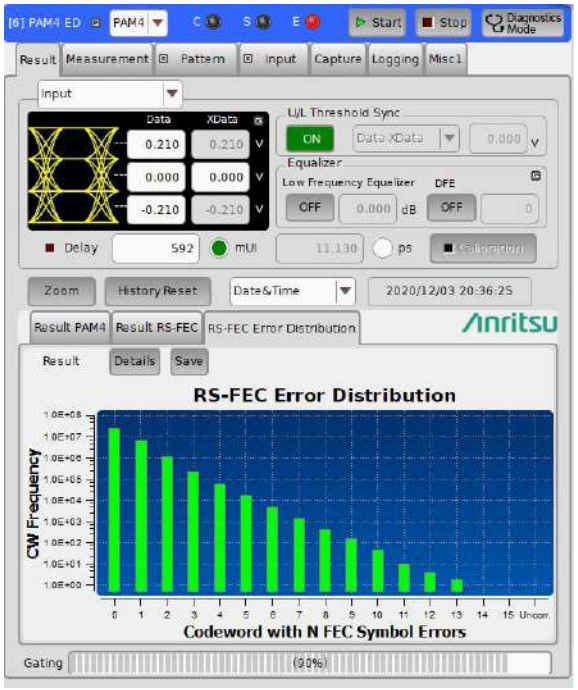
Sample Video

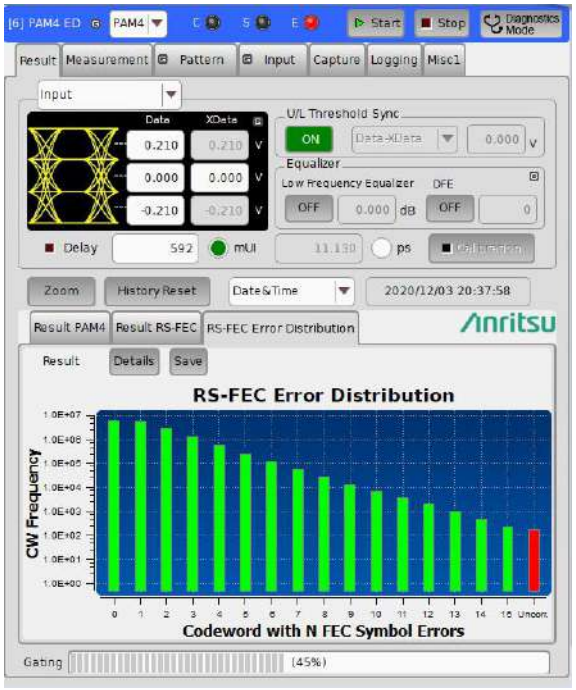
Error Free



Correctable Errors



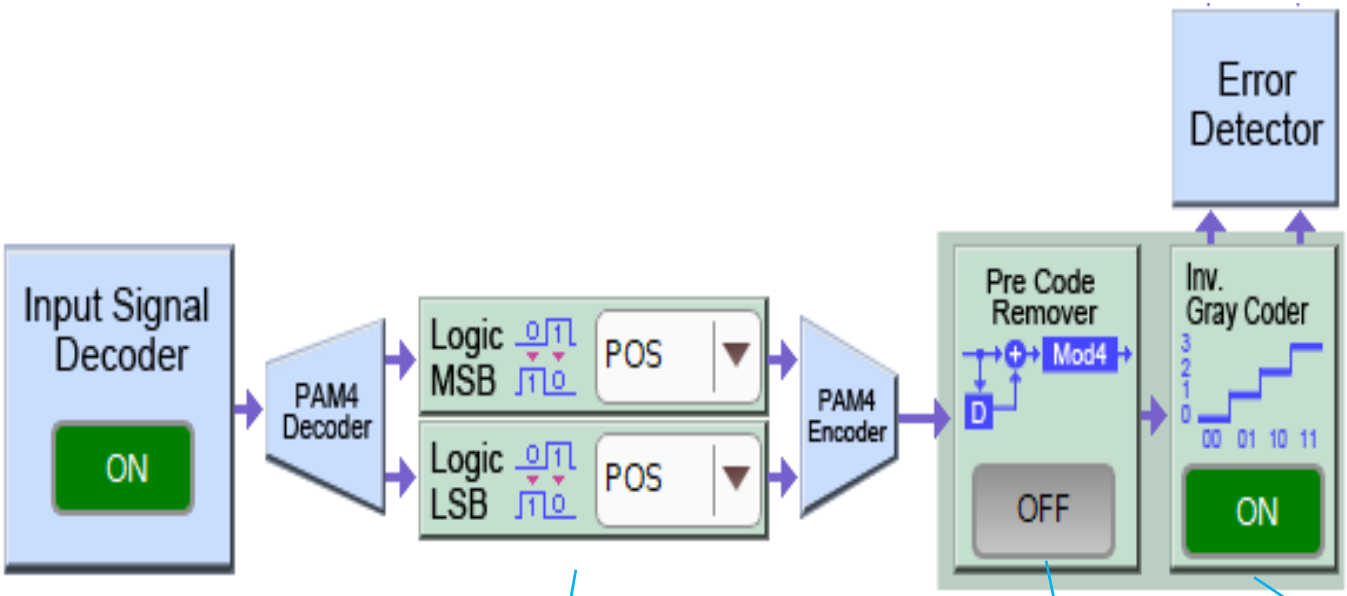
Uncorrectable Errors



Stress Injection

Decoding Function

Supports Gray decode function
Decodes input data and measures FEC Symbol Errors



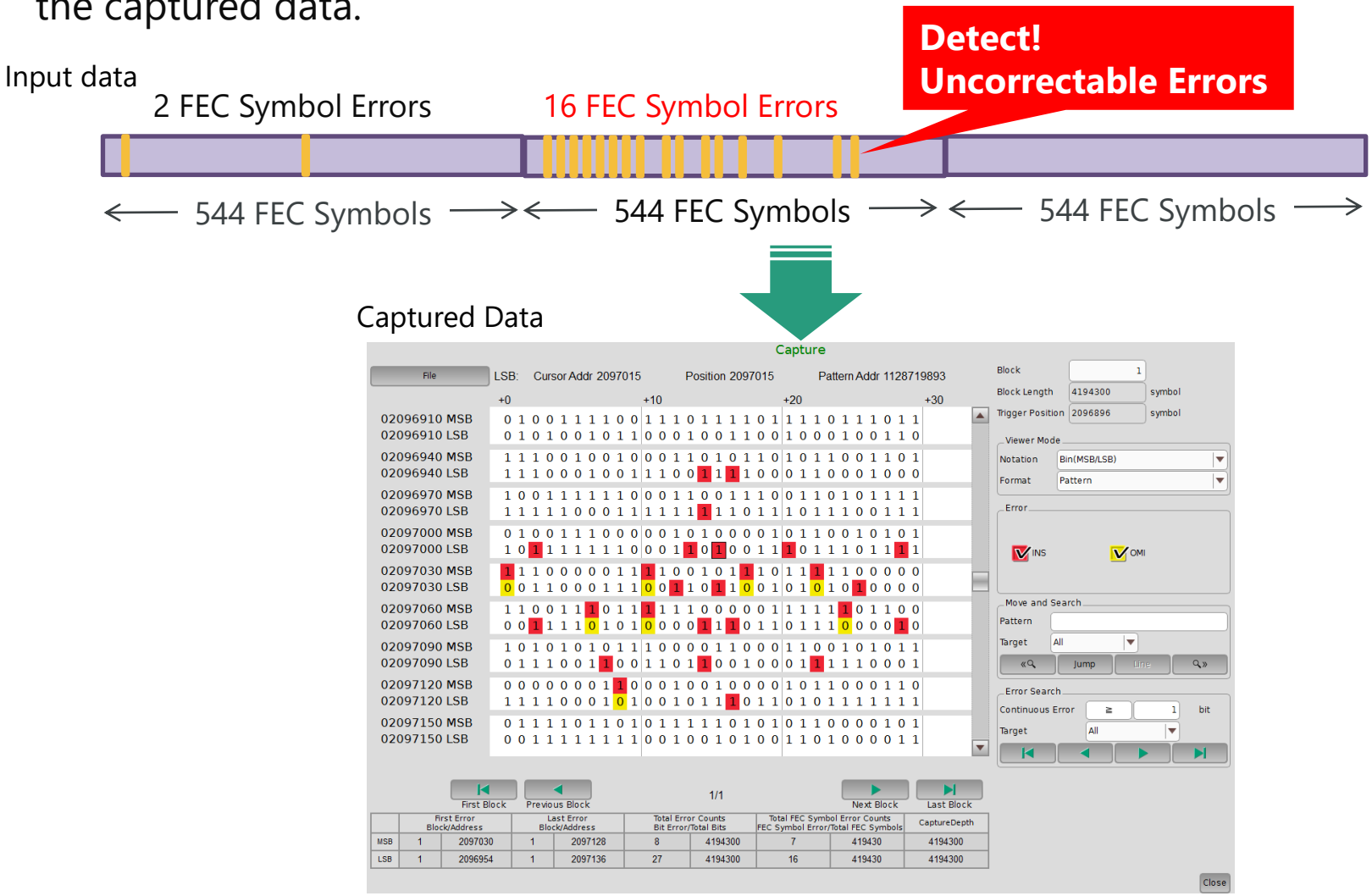
MSB and LSB Inverted Logic (before/after Gray Coding)

1/(1+D) Mod4 Decoding

Gray Decoding

FEC Symbol Capture

The input data is captured when the number of FEC Symbol Errors exceeds the threshold setting. The causes of FEC-uncorrectable errors can be analyzed from the captured data.



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